



**WINSTAR Display Co.,Ltd.**  
**華凌光電股份有限公司**



# Winstar Display Co., LTD

## 華凌光電股份有限公司



WEB: <https://www.winstar.com.tw> E-mail: [sales@winstar.com.tw](mailto:sales@winstar.com.tw)

### SPECIFICATION

**CUSTOMER :** \_\_\_\_\_

**MODULE NO.:** WF80GSYAUMNGO#

<p><b>APPROVED BY:</b> ( FOR CUSTOMER USE ONLY )</p>	<p><b>PCB VERSION:</b> _____ <b>DATA:</b> _____</p>
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SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
			葉虹蘭
<b>ISSUED DATE: 2024/12/31</b>			

TFT Display Inspection Specification: <https://www.winstar.com.tw/technology/download.html>

Precaution in use of TFT module: <https://www.winstar.com.tw/technology/download/declaration.html>

MODLE NO :

<b>RECORDS OF REVISION</b>	<b>DOC. FIRST ISSUE</b>
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VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2023/10/11		First issue
A	2024/12/31		Modify Static electricity test Modify Initial Code For Reference

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# 1.Module Classification Information

W F 80 G S Y A U M N G 0 #  
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪ ⑫ ⑬

①	Brand : WINSTAR DISPLAY CORPORATION											
②	Display Type : F→TFT Type, J→Custom TFT											
③	Display Size : 8.0" TFT											
④	Model serials no.											
⑤	Backlight Type :	F→CCFL, White S→LED, High Light White					T→LED, White Z→Nichia LED, White					
⑥	LCD Polarize Type/ Temperature range/ Gray Scale Inversion Direction	A→Transmissive, N.T, IPS TFT C→Transmissive, N. T, 6:00 ; F→Transmissive, N.T,12:00 ; I→Transmissive, W. T, 6:00 K→Transflective, W.T,12:00 L→Transmissive, W.T,12:00 N→Transmissive, Super W.T, 6:00					Q→Transmissive, Super W.T, 12:00 R→Transmissive, Super W.T, O-TFT V→Transmissive, Super W.T, VA TFT W→Transmissive, Super W.T, IPS TFT X→Transmissive, W.T, VA TFT Y→Transmissive, W.T, IPS TFT Z→Transmissive, W.T, O-TFT					
⑦	A : TFT LCD B : TFT+SCREW HOLES+CONTROL BOARD C : TFT+ SCREW HOLES +A/D BOARD D : TFT+ SCREW HOLES +A/D BOARD+CONTROL BOARD E : TFT+ SCREW HOLES +POWER BOARD					F : TFT+CONTROL BOARD G : TFT+ SCREW HOLES H : TFT+D/V BOARD I : TFT+ SCREW HOLES +D/V BOARD J : TFT+POWER BD						
⑧	Resolution:											
	A	128160	B	320234	C	320240	D	480234	E	480272	F	640480
	G	800480	H	1024600	I	320480	J	240320	K	800600	L	240400
	M	1024768	N	128128	P	1280800	Q	480800	R	640320	S	480128
	T	800320	U	8001280	V	176220	W	1280398	X	1024250	Y	1920720
	Z	800200	2	1024324	3	7201280	4	19201200	5	1366768	6	1280320
⑨	D: Digital L : LVDS M:MIPI											
⑩	Interface:											
	N	Without control board			A	8Bit	B	16Bit		H	HDMI	
	I	I2C Interface			R	RS232	S	SPI Interface		U	USB	
⑪	TS:											
	N	Without TS			T	Resistive touch panel			C	Capacitive touch panel (G-F-F)		
	G	Capacitive touch panel (G-G)					C1	Capacitive touch panel (G-F-F)+OCA				
	C2	Capacitive touch panel (G-F-F)+OCR					G1	Capacitive touch panel (G-G)+OCA				
	G2	Capacitive touch panel (G-G)+OCR					B	CTP+GG+USB				
⑫	Version: X:Raspberry pi											
⑬	Special Code	#:Fit in with ROHS directive regulations										

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## **2.Summary**

TFT 8.0“ is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This TFT LCD has a 8.0 (10:16) inch diagonally measured active display area with WXGA (800 horizontal by 1280 vertical pixel) resolution.

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### 3. General Specifications

Item	Dimension	Unit
Size	8.0	inch
Dot Matrix	800× 3(RGB) ×1280	dots
Module dimension	123.74 × 192.08 × 7.95	mm
Active area	107.64 × 172.224	mm
Pixel pitch	0.13455 x 0.13455	mm
LCD type	TFT, Normally Black, Transmissive	
Viewing angle	85/85/85/85	
TFT Drive IC	ILI9881C or Equivalent	
TFT Interface	4-Lanes MIPI	
Aspect Ratio	10:16	
Backlight Type	LED ,Normally White	
CTP FW Version	0x07.0x00.0x00.0x00.0x01.0x00.0x83.0x65	
CTP interface	I2C	
CTP IC	ILI2130 or equivalent	
CTP Resolution	16384 * 16384	
With /Without TP	With CTP	
Surface	Glare	

\*Color tone slight changed by temperature and driving voltage.

## 4. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	°C
Storage Temperature	TST	-30	—	+80	°C

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp.  $\leq 60^{\circ}\text{C}$ , 90% RH MAX. Temp.  $> 60^{\circ}\text{C}$ , Absolute humidity shall be less than 90% RH at  $60^{\circ}\text{C}$

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# 5. Electrical Characteristics

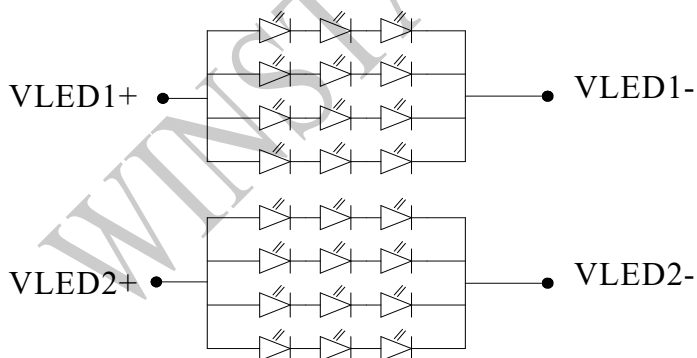
## 5.1. Typical Operation Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power supply for analog circuit	VCI	3.0	3.3	3.6	V	
Power supply for logic circuit	IOVCC	1.65	1.8	3.6	V	
Current for Driver	I <sub>VCI</sub>	-	45	70	mA	VCI= 3.3V
	I <sub>IOVCC</sub>	-	20	30	mA	IOVCC=1.8V
Supply CTP	+3.3	3.15	3.3	3.45	V	
	+3.3V	-	70	100	mA	

## 5.2. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current for VLED1+	I <sub>LED1</sub>	-	240	-	mA	
LED voltage for VLED1+	V <sub>LED1</sub>	8.1	9.0	10.2	V	Note 1
LED current for VLED2+	I <sub>LED2</sub>	-	240	-	mA	
LED voltage for VLED2+	V <sub>LED2</sub>	8.1	9.0	10.2	V	Note 1
LED Life Time		-	50,000	-	Hr	Note 2,3,4

Note 1 : There are 1 Groups LED



## CIRCUIT DIAGRAM

Note 2 : Ta = 25 °C

Note 3 : Brightness to be decreased to 50% of the initial value

Note 4 : The single LED lamp case

# 6.DC CHARATERISTICS

## 6.1. Basic Characteristics for Panel Driving

Parameter	Symbol	Rating			Unit	Condition	Note
		Min	Typ	Max			
Logic Low level input voltage	$V_{IL}$	-0.3	-	$0.3 \cdot IOVCC$	V		Note1
Logic High level input voltage	$V_{IH}$	$0.7 \cdot IOVCC$	-	$IOVCC$	V		Note1
Logic Low level output voltage (TE)	$V_{OL}$	0		$0.2 \cdot IOVCC$	V	$I_{OL} = +1.0mA$	Note1
Logic High level output voltage (TE)	$V_{OH}$	$0.8 \cdot IOVCC$		$IOVCC$	V	$I_{OH} = -1.0mA$	Note1

NOTE1:

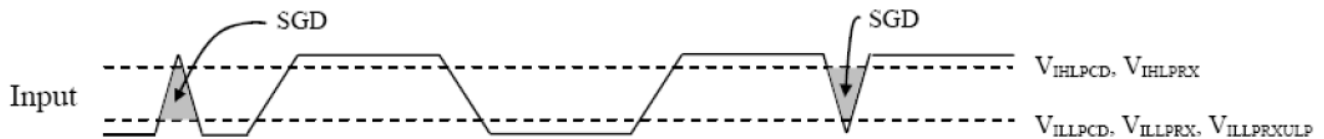
$T_a = -20$  to  $70^\circ C$ ,  $V_{CI} = 3.3V$ ,  $IOVCC = 1.8V$

## 6.2. DSI DC Characteristics

LP Mode

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	$V_{IHLPCD}$	LP-CD	450	-	1350	mV
Logic 0 input voltage	$V_{ILLPCD}$	LP-CD	0.0	-	200	mV
Logic 1 input voltage	$V_{IHLPRX}$	LP-RX (CLK, D0, D1, D2, D3)	880	-	1350	mV
Logic 0 input voltage	$V_{ILLPRX}$	LP-RX (CLK, D0, D1, D2, D3)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	$V_{OHLPTX}$	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	$V_{OLLPTX}$	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	$I_{IH}$	LP-CD, LP-RX	-	-	10	$\mu A$
Logic 0 input current	$I_{IL}$	LP-CD, LP-RX	-10	-	-	$\mu A$

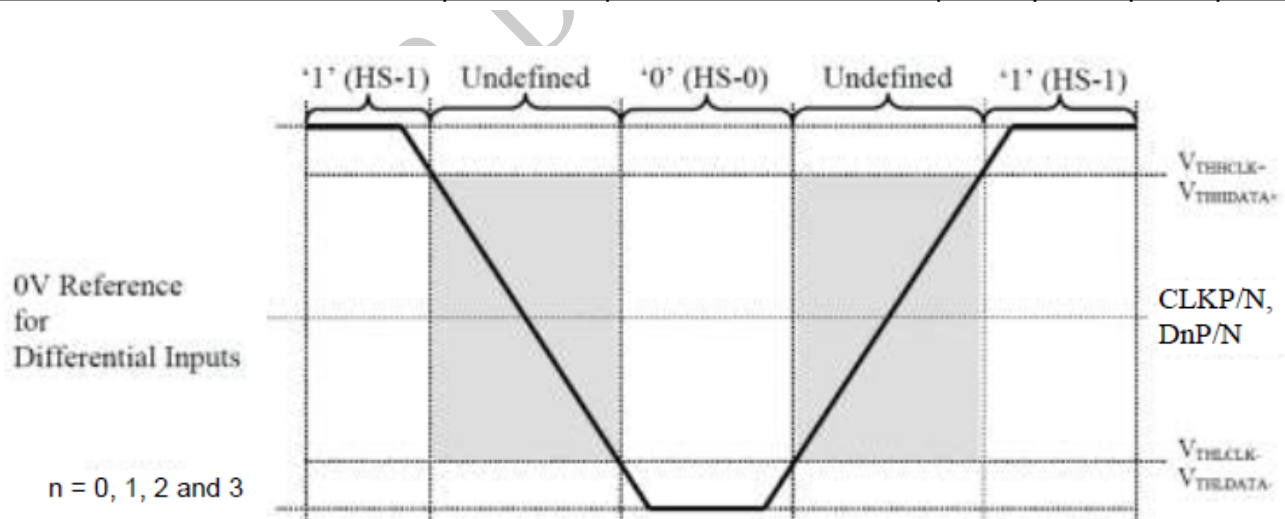
Spike/Glitch Rejection

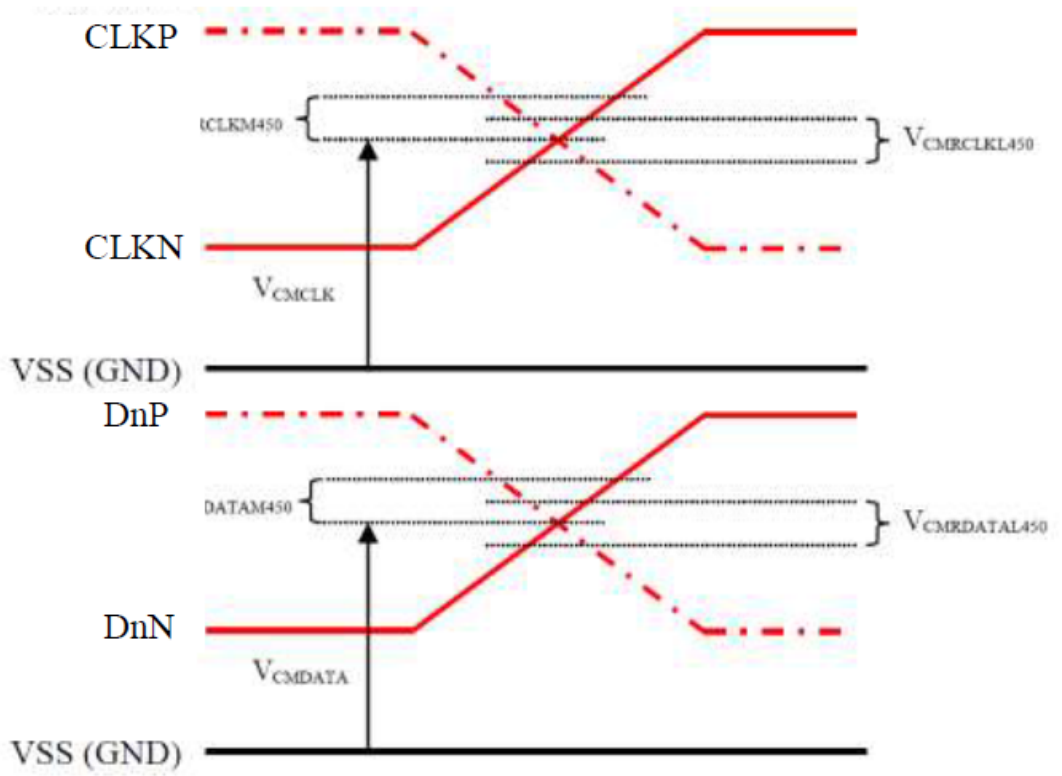


Spike/Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N, DnP/N	SGD	Input pulse rejection for DSI	-	300	Vps

## High Speed Mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	$V_{CMCLK}$	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	$V_{CMDATA}$	DnP/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLK450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DnP/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DnP/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N Note 5	-	-	70	mV
Single-ended Input Low Voltage	$V_{ILHS}$	CLKP/N, DnP/N Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	$V_{IHHS}$	CLKP/N, DnP/N Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	$R_{TERM}$	CLKP/N, DnP/N Note 5	80	100	125	$\Omega$
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, DnP/N Note 5	-	-	450	mV
Termination Capacitor	$C_{TERM}$	CLKP/N, DnP/N Note 5, Note 6	-	-	60	pF





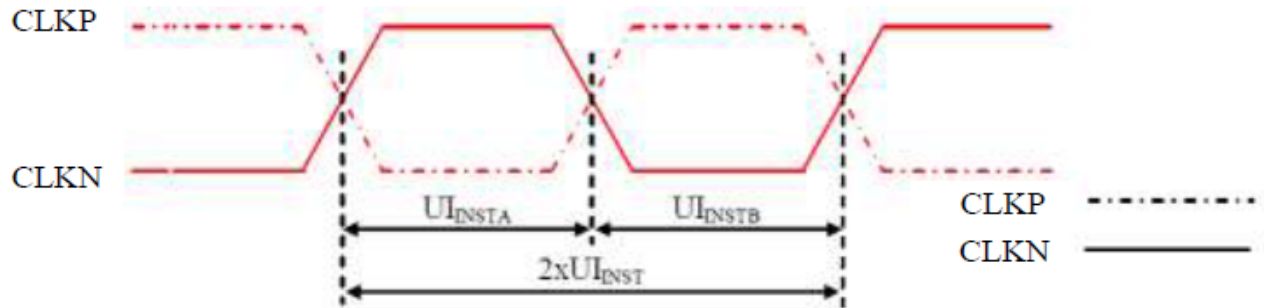
Note:  $n = 0, 1, 2$  and  $3$

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# 7.AC Characteristics

## 7.1. DSI Interface Timing Characteristics

### 7.1.1 High Speed Mode – Clock Channel Timing



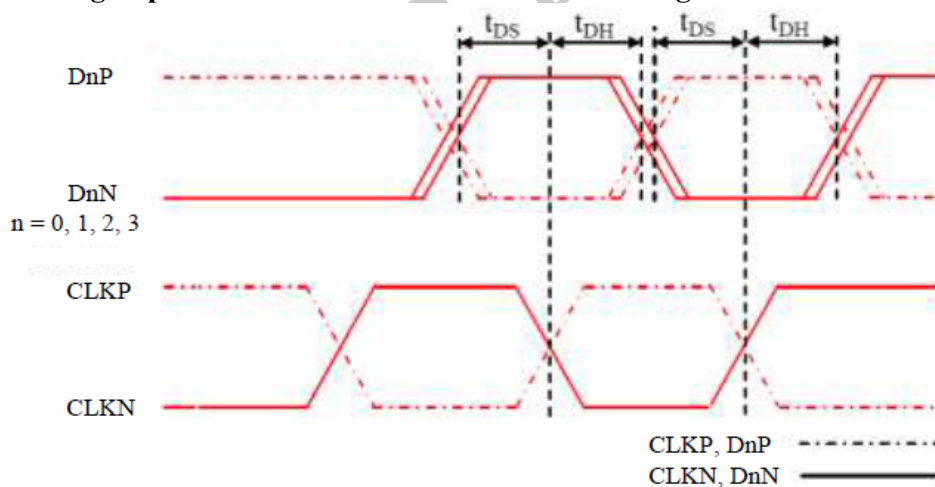
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	Note 2	25	ns
CLKP/N	$UI_{INSTA}, UI_{INSTB}$ (Note 1)	UI instantaneous Half	Note 2	12.5	ns

Notes:

1.  $UI = UI_{INSTA} = UI_{INSTB}$

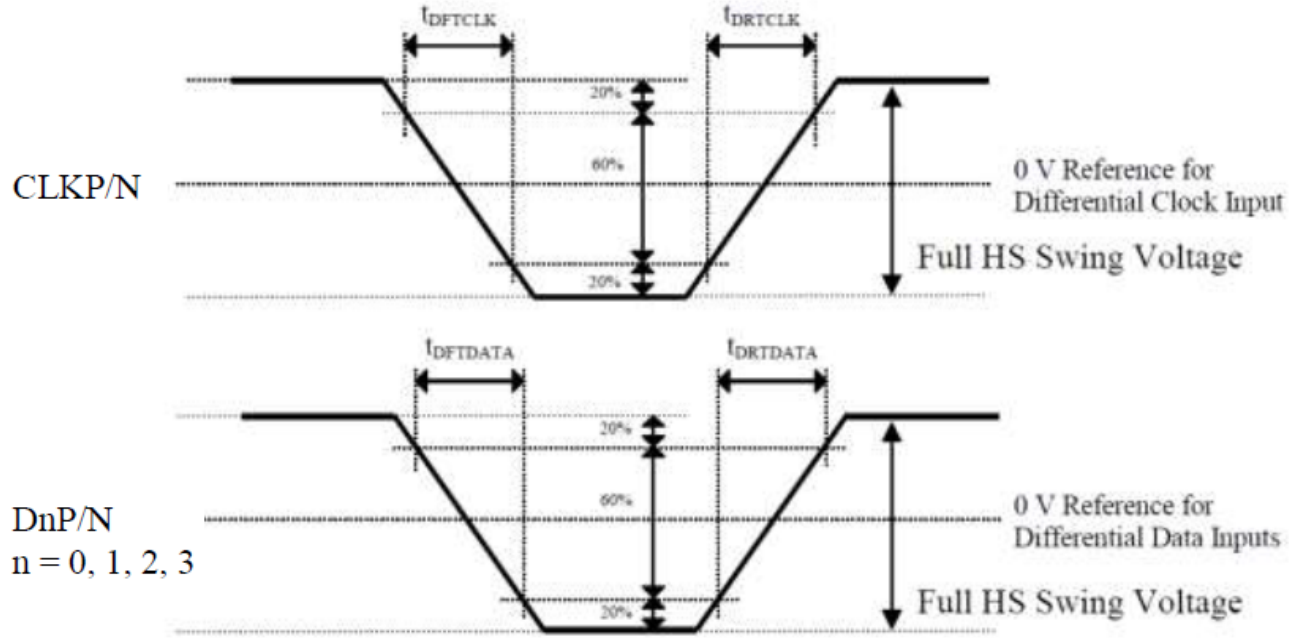
Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

### 7.1.2 High Speed Mode – Data Clock Channel Timing



Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	$t_{DS}$	Data to Clock Setup time	$0.15xUI$	-
	$t_{DH}$	Clock to Data Hold Time	$0.15xUI$	-

### 7.1.3 High Speed Mode – Rising and Falling Timings



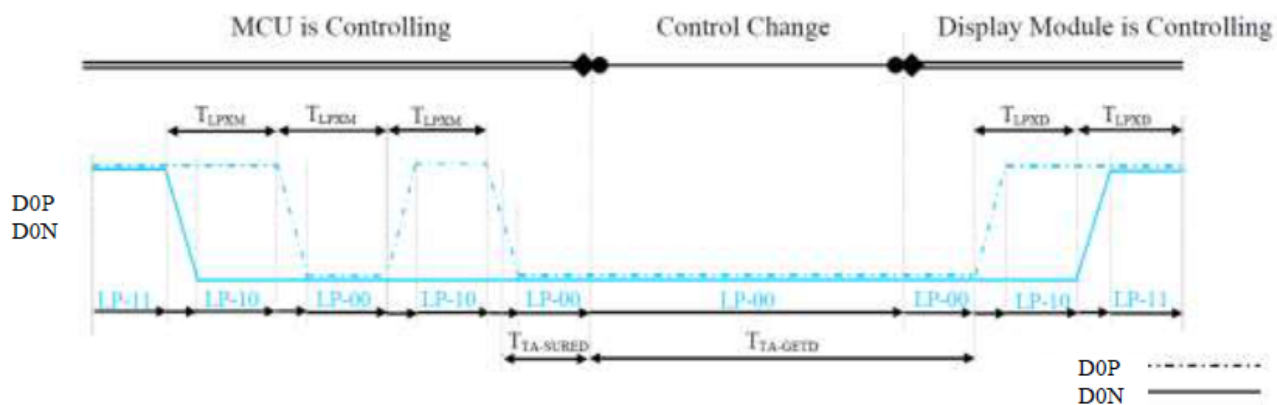
**Table 41: Rise and Fall Timings on Clock and Data Channels**

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	$t_{DRTCLK}$	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	$t_{DFTCLK}$	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

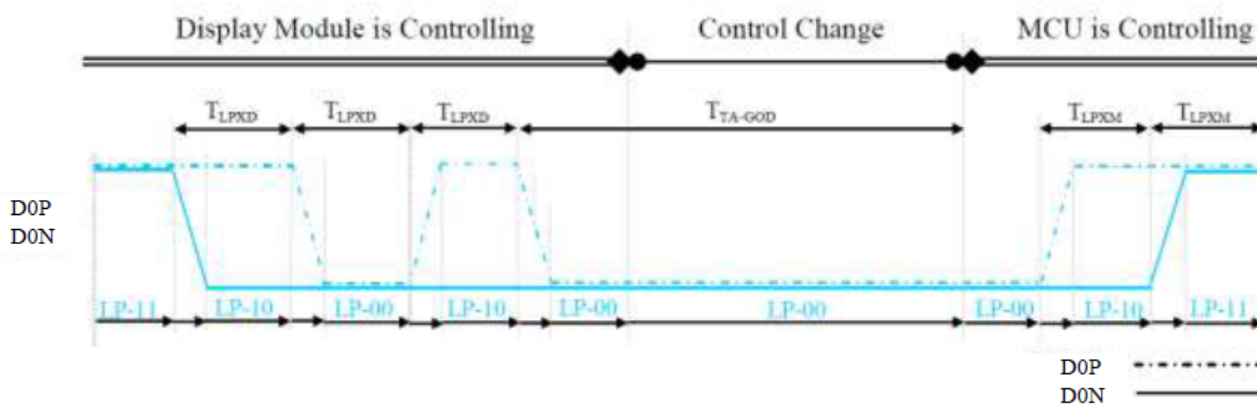
**Note:** The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

WINSI

### 7.1.4 Low Power Mode – Bus Turn Around



**BTA from the MCU to Display Module**

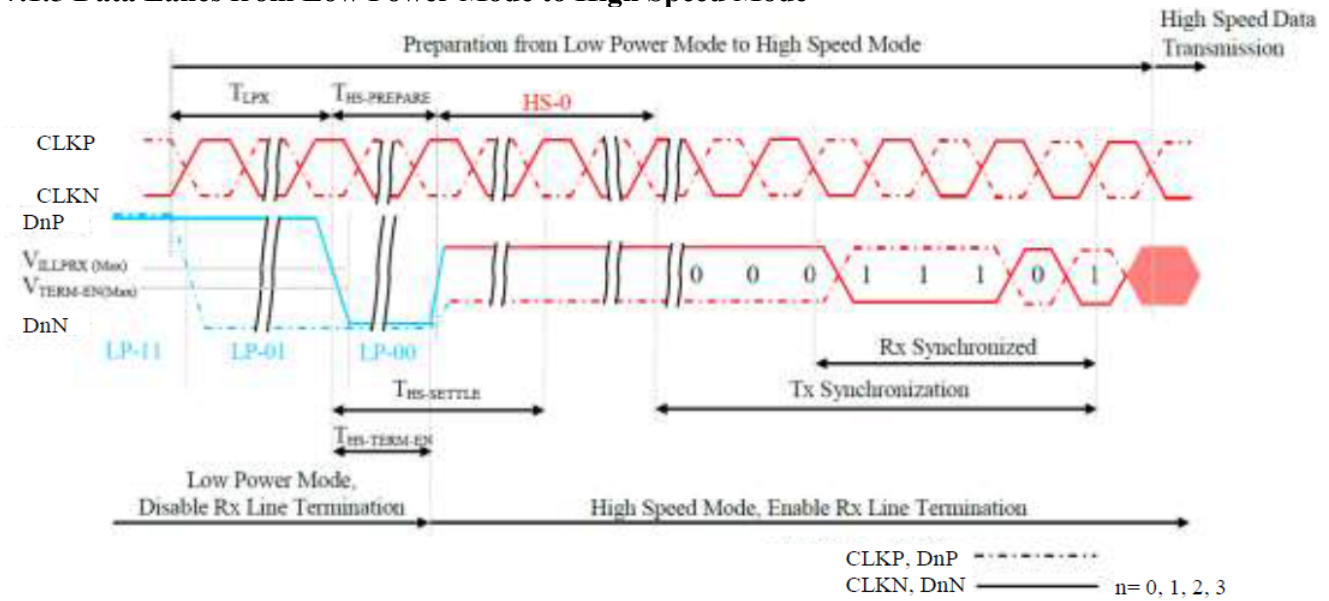


**BTA from Display Module to the MCU**

Signal	Symbol	Description	Min	Max	Unit
D0P/N	$T_{LPXM}$	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	$T_{LPXD}$	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	$T_{LPXD}$	$2 \times T_{LPXD}$	ns

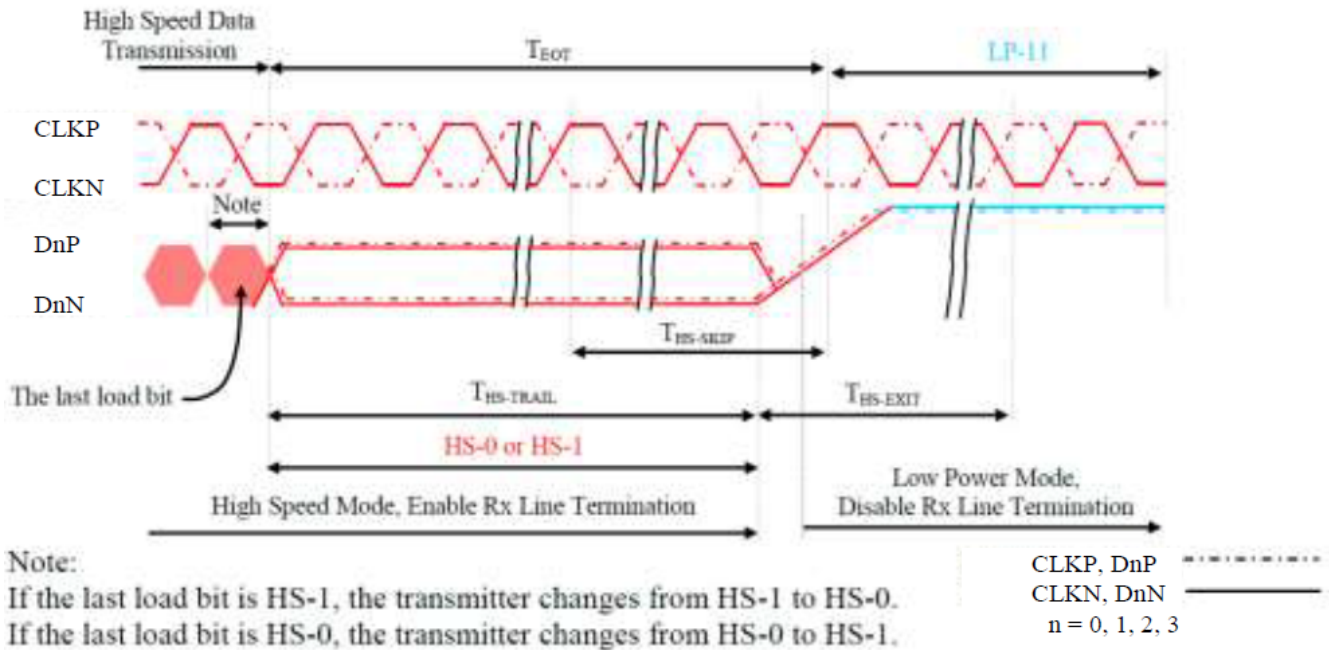
Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5 \times T_{LPXD}$	ns
D0P/N	$T_{TA-GOD}$	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LPXD}$	ns

### 7.1.5 Data Lanes from Low Power Mode to High Speed Mode



Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{LPX}$	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	$40+4xUI$	$85+6xUI$	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses $V_{ILMAX}$	-	$35+4xUI$	ns

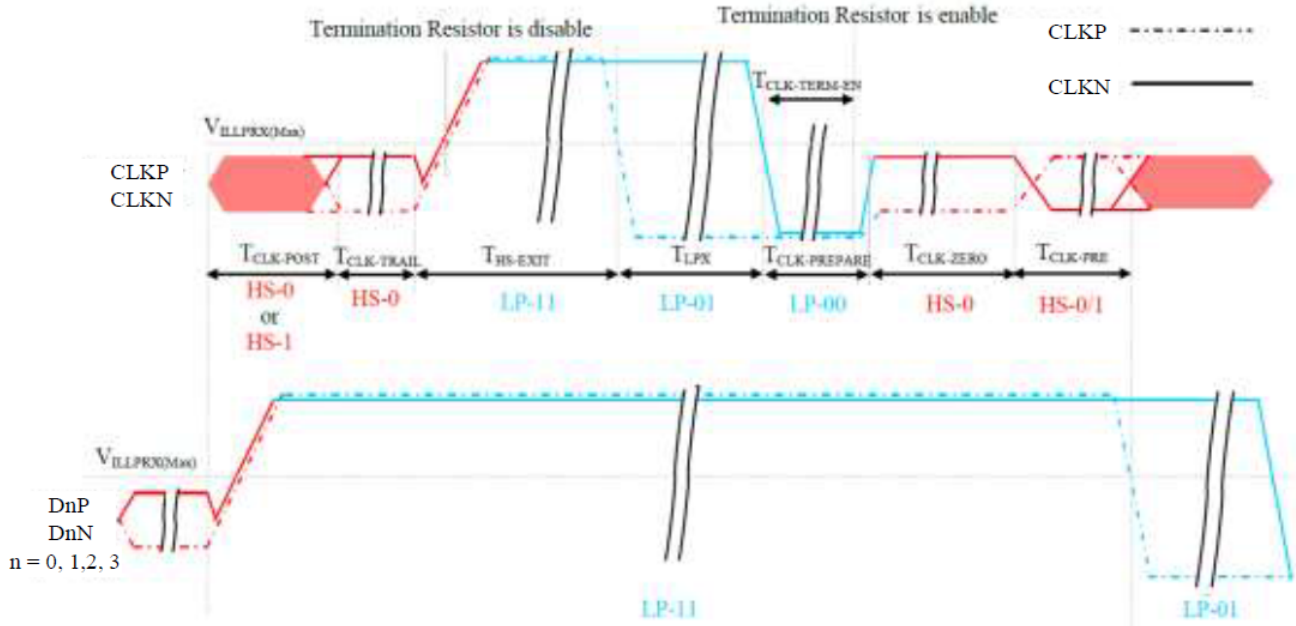
### 7.1.6 Data Lanes from High Speed Mode to Low Power Mode



Note:  
 If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.  
 If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

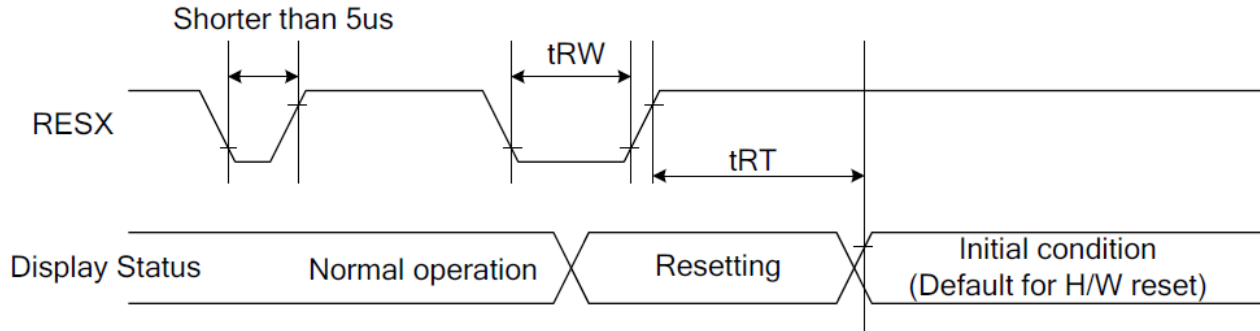
Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	$55+4xUI$	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

### 7.1.7 Clock Lanes High Speed Mode to/from Low Power Mode Timing



Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	$60+52xUI$	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$8xUI$	-	ns

## 7.2. Reset Timing



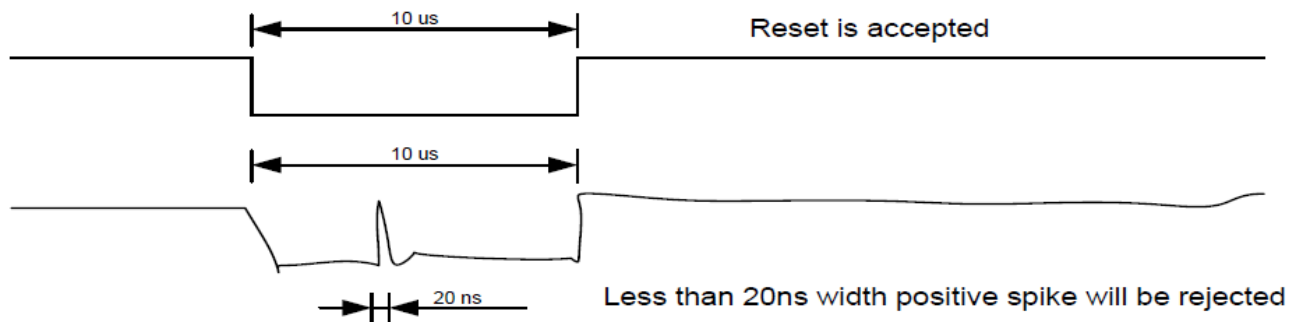
Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5 (Note 1, 5) 120 (Note 1, 6, 7)	ms

### Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

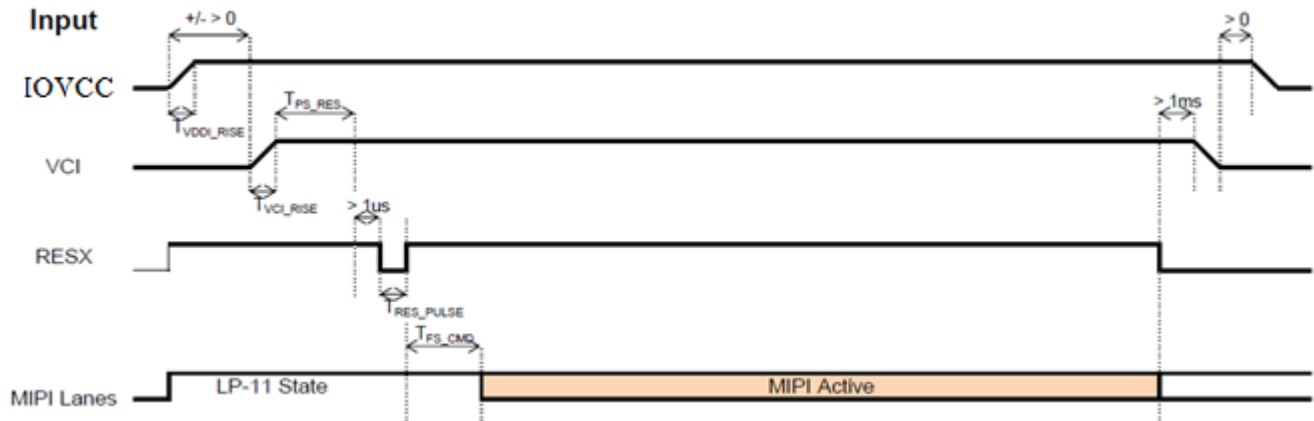
3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



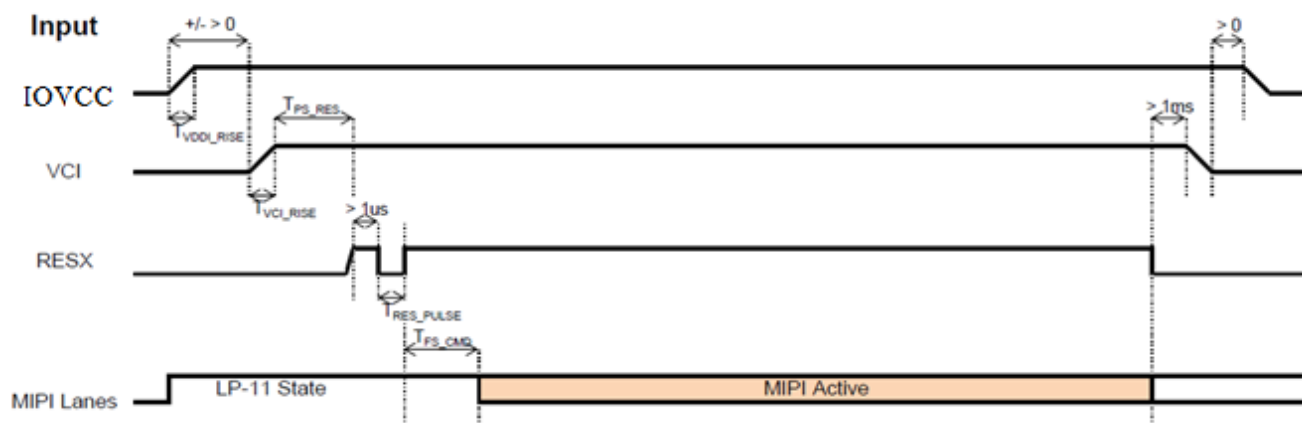
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

# 8. Power ON/OFF Sequence

Case A:



Case B:



Symbol	Characteristics	Min.	Typ.	Max.	Units
$T_{IOVCC\_RISE}$	IOVCC Rise time	10	-	-	us
$T_{VCI\_RISE}$	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40	-	-	us
$T_{PS\_RES}$	VDDI/VCI on to Reset high	5	-	-	ms
$T_{RES\_PULSE}$	Reset low pulse time	10	-	-	us
$T_{FS\_CMD}$	Reset to first command	10	-	-	ms

# 9. Optical Characteristics

Item	Symbol	Condition.	Min	Typ.	Max.	Unit	Remark	
Response time	Tr+ Tf	$\theta=0^\circ$ 、 $\Phi=0^\circ$	-	30	35	.ms	Note 3	
Contrast ratio	CR	At optimized viewing angle	1200	1500	-	-	Note 4	
Color Chromaticity	White	Wx	$\theta=0^\circ$ 、 $\Phi=0$	0.248	0.298	0.348	Note 2,6,7	
		Wy		0.274	0.324	0.374		
Viewing angle	Hor.	$\Theta_R$	$CR \geq 10$	80	85	-	Deg.	Note 1
		$\Theta_L$		80	85	-		
	Ver.	$\Phi_T$		80	85	-		
		$\Phi_B$		80	85	-		
Brightness	-	-	800	900	-	cd/m <sup>2</sup>	Center of display	
Uniformity	(U)	-	70	-	-	%	Note 5	

Ta=25±2°C, (ILED2=240mA & ILED1=240mA)

Note 1: Definition of viewing angle range

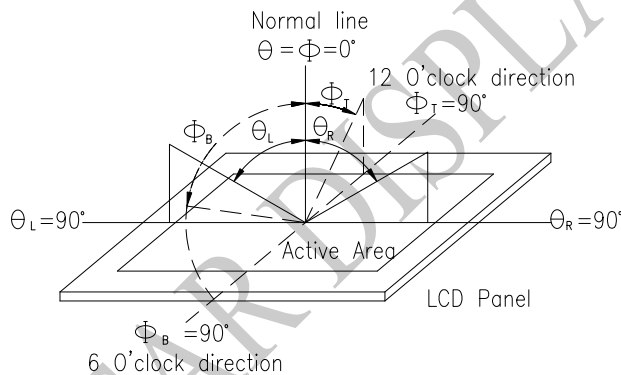


Fig. 9.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7or BM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

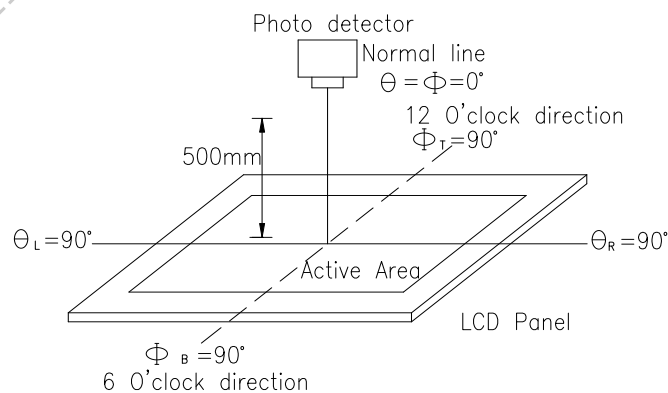
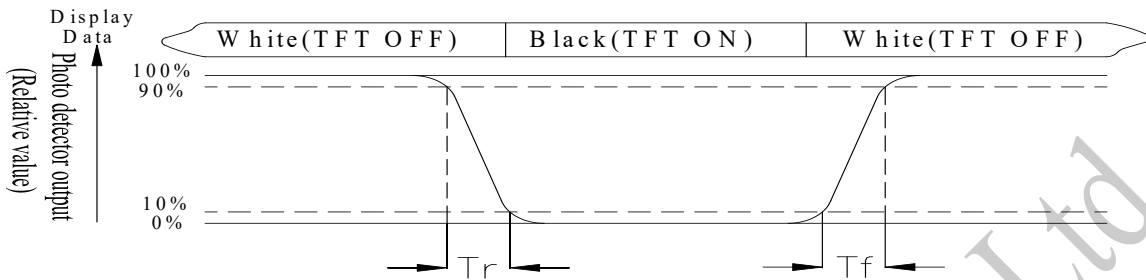


Fig. 9.2. Optical measurement system setup

**Note 3: Definition of Response time:**

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time,  $T_r$ , is the time between photo detector output intensity changed from 90% to 10%. And fall time,  $T_f$ , is the time between photo detector output intensity changed from 10% to 90%



**Note 4: Definition of contrast ratio:**

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

**Note 5: Definition of Luminance Uniformity**

Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (U)} = \text{Lmin/Lmax} \times 100\%$$

L = Active area length

W = Active area width

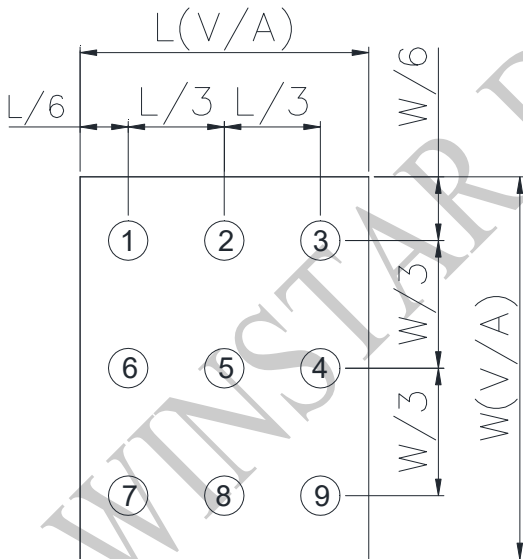


Fig 9.3. Definition of uniformity

**Note 6: Definition of color chromaticity (CIE 1931)**

Color coordinates measured at the center point of LCD

**Note 7:** Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

# 10.Interface

## 10.1. LCM PIN Definition

Pin	Symbol	Function	Remark
1-9	NC	No connection	
10-11	VCI	Power supply for analog circuits. Connect to an external power supply of 3.0V to 3.6V	
12-13	NC	No connection	
14	RESET	The external reset input (RESX) Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power. Fix to IOVCC level when not in use.	
15	TE	Tearing effect output pin. Leave the pin open when not in use.	
16	NC	No connection (LED PWM)	
17-18	GND	Power ground	
19-20	IOVCC	Power supply for analog circuits. Connect to an external power supply of 1.65V to 3.6V	
21	GND	Power ground	
22	D3P	MIPI DSI differential data pair. (Data lane 3)	
23	D3N		
24	GND	Power ground	
25	D2P	MIPI DSI differential data pair. (Data lane 2)	
26	D2N		
27	GND	Power ground	
28	CLKP	MIPI DSI differential clock pair	
29	CLKN		
30	GND	Power ground	
31	D1P	MIPI DSI differential data pair. (Data lane 1)	
32	D1N		
33	GND	Power ground	
34	D0P	MIPI DSI differential data pair. (Data lane 0)	
35	D0N		
36	GND	Power ground	
37	VLED1+	Power for LED1 backlight anode	
38	VLED2+	Power for LED2 backlight anode	
39	VLED1-	Power for LED1 backlight cathode	

40	VLED2-	Power for LED2 backlight cathode	
----	--------	----------------------------------	--

## 10.2. CTP PIN Definition

Pin	Symbol	Function	Remark
1	VSS	Ground for analog circuit	
2	VDDT	Power Supply : +3.3V	
3	SCL	I2C clock input	
4	NC	No connection	
5	SDA	I2C data input and output	
6	NC	No connection	
7	/RST	External Reset, Low is active	
8	NC	No connection	
9	/INT	External interrupt to the host	
10	VSS	Ground for analog circuit	

WINSTAR DISPLAY Co., Ltd.

# 11. Reliability

Content of Reliability Test (Wide temperature, -20°C~70°C)

Environmental Test			
Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 240hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 240hrs	2
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 240hrs	1,2
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max	60°C,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation <div style="text-align: center;"> <p style="margin: 0;">-20°C    25°C    70°C</p> <p style="margin: 0;">30min    5min    30min</p> <p style="margin: 0;">1 cycle</p> </div>	-20°C/70°C 10 cycles	2
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±4KV(contact), ±4KV(air), RS=330Ω CS=150pF 10 times	4

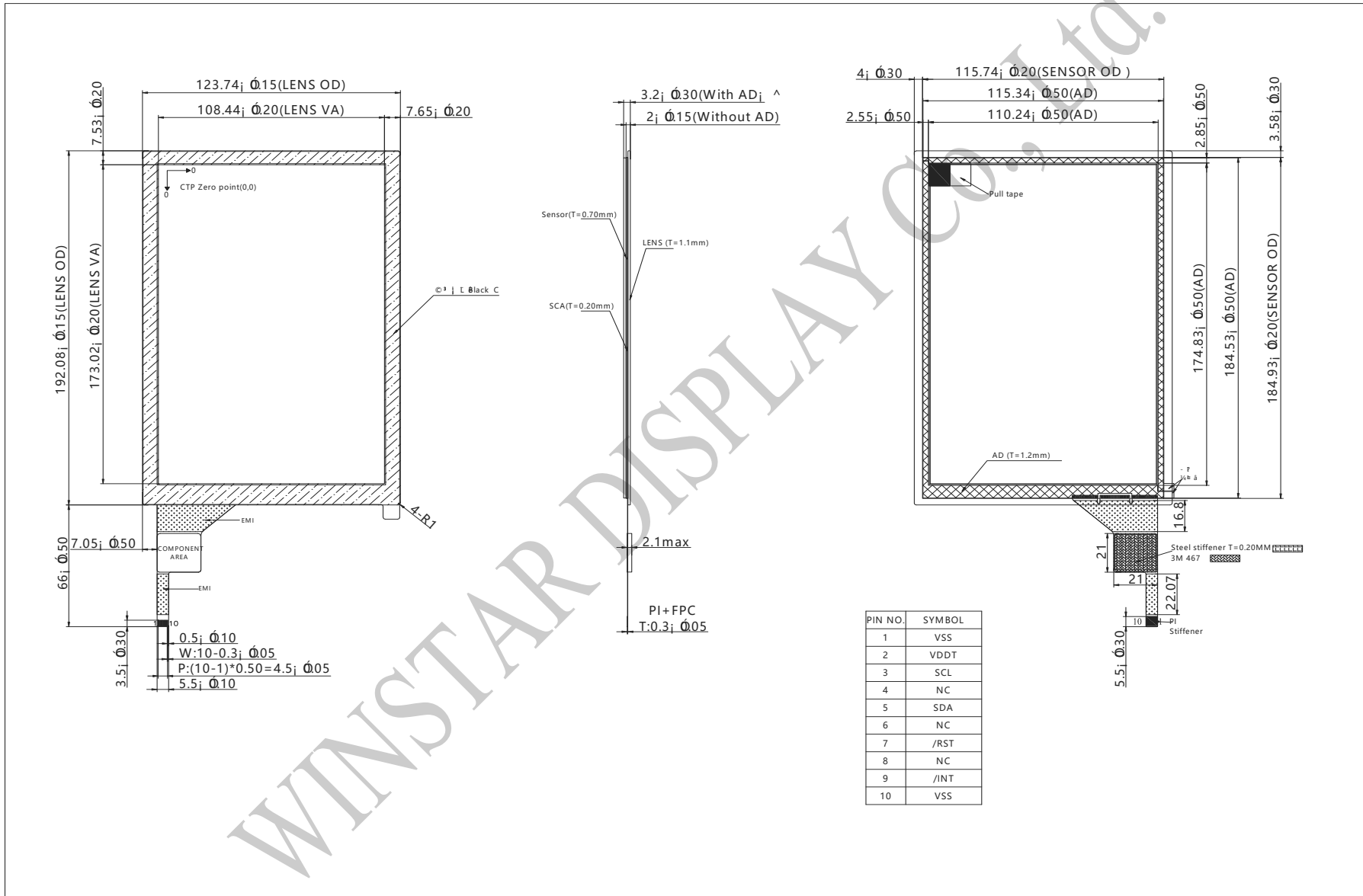
Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

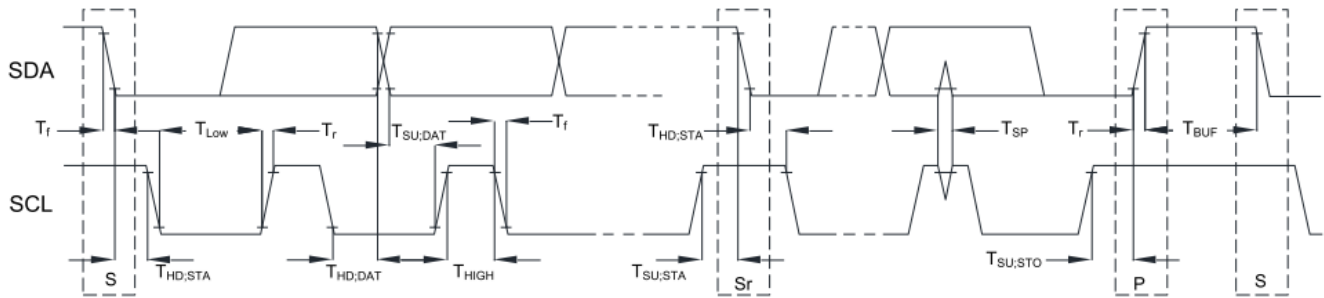
Note3: The packing have to including into the vibration testing.

Note4: Endurance test applying the electric stress to the finished product housing

# 12.Touch Panel Information

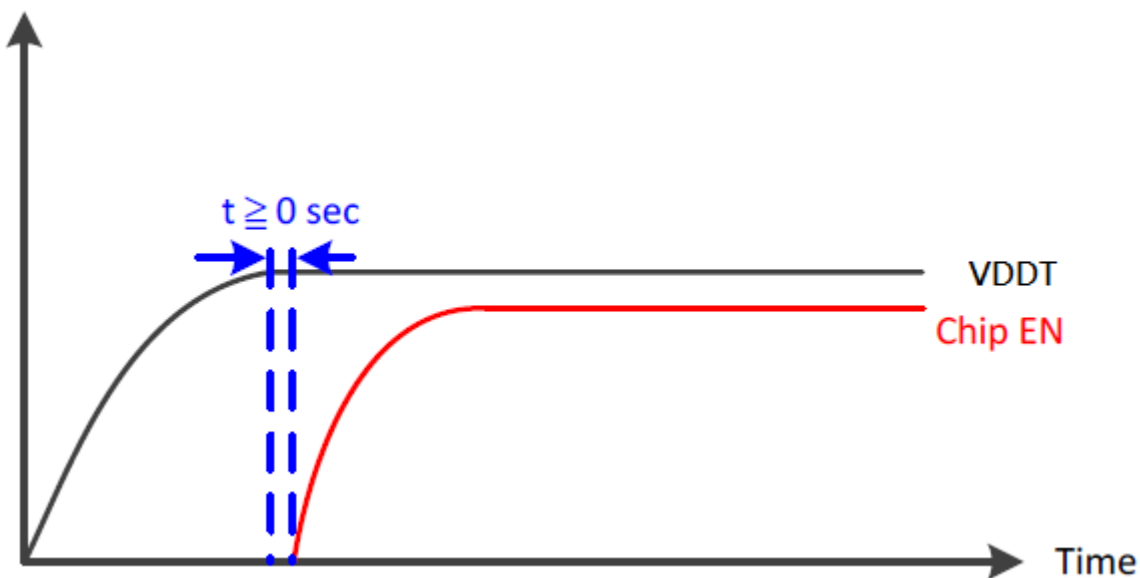


## 12.1. I2C AC Characteristics

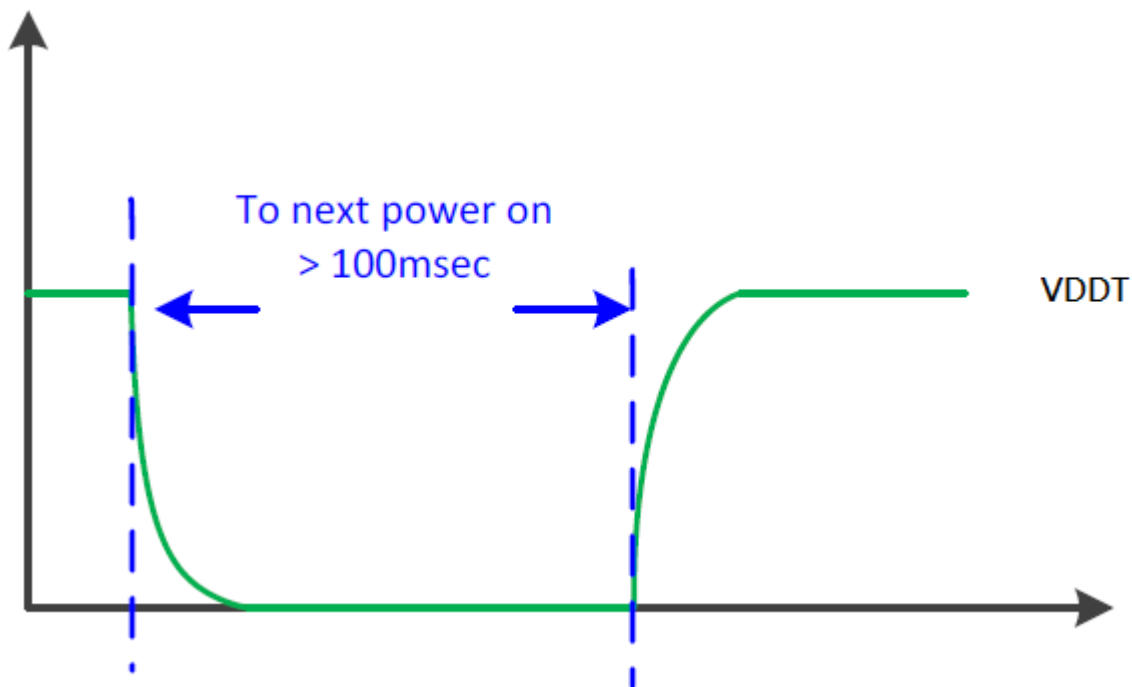


Item	Symbol	100kHz		400kHz		Unit
		Min.	Max.	Min.	Max.	
SCL standard mode clock frequency	F <sub>SCL</sub>	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock is generated.	T <sub>HD;STA</sub>	4	--	0.6	--	us
LOW period of the SCL clock	T <sub>LOW</sub>	4.7	--	1.3	--	us
HIGH period of the SCL clock	T <sub>HIGH</sub>	4	--	0.6	--	us
Setup time for a repeat START condition.	T <sub>SU;STA</sub>	4.7	--	0.6	--	us
Data hold time	T <sub>HD;DAT</sub>	0	3.45	0	0.9	us
Data setup time	T <sub>SU;DAT</sub>	250	--	100	--	ns
Rising time of both SDA and SCL signals	T <sub>r</sub>	--	1000	--	300	ns
Falling time of both SDA and SCL signals	T <sub>f</sub>	--	300	--	300	ns
Setup time for STOP condition.	T <sub>SU;STO</sub>	4	--	0.6	--	us
Free time between STOP and START condition	T <sub>BUF</sub>	4.7	--	1.3	--	us
Pulse width of spikes which must be suppressed by input filter	T <sub>SP</sub>	--	--	0	50	ns

## 12.2. Power On Sequence

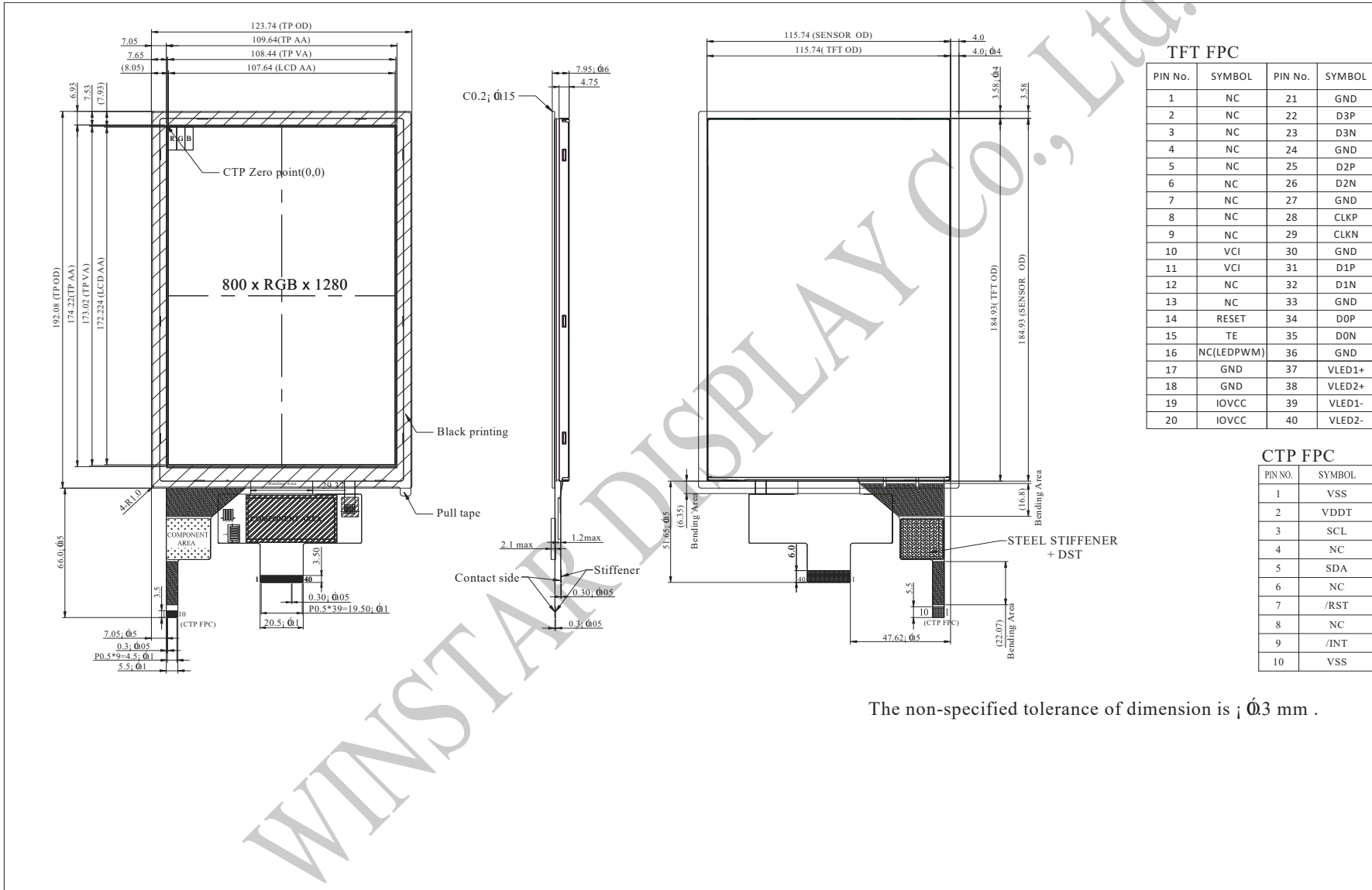


### 12.3. Power Off to Power On Sequence



WINSTAR DISPLAY

# 13. Contour Drawing



TFT FPC

PIN No.	SYMBOL	PIN No.	SYMBOL
1	NC	21	GND
2	NC	22	D3P
3	NC	23	D3N
4	NC	24	GND
5	NC	25	D2P
6	NC	26	D2N
7	NC	27	GND
8	NC	28	CLKP
9	NC	29	CLKN
10	VCI	30	GND
11	VCI	31	D1P
12	NC	32	D1N
13	NC	33	GND
14	RESET	34	DOP
15	TE	35	DON
16	NC(LED PWM)	36	GND
17	GND	37	VLED1+
18	GND	38	VLED2+
19	IOVCC	39	VLED1-
20	IOVCC	40	VLED2-

CTP FPC

PIN NO.	SYMBOL
1	VSS
2	VDDT
3	SCL
4	NC
5	SDA
6	NC
7	/RST
8	NC
9	/INT
10	VSS

The non-specified tolerance of dimension is ; ±0.3 mm .

# 14.Initial Code For Reference

ILI9881C\_HSD\_80G

REGISTER,FF,03,98,81,03

//GIP\_1

REGISTER,01,01,00

REGISTER,02,01,00

REGISTER,03,01,53

//STVA Width 4H

REGISTER,04,01,13

//STVB Width 4H

REGISTER,05,01,00

REGISTER,06,01,04

//STVA Rise start

REGISTER,07,01,00

//STVB Rise start

REGISTER,08,01,00

REGISTER,09,01,20

REGISTER,0A,01,20

REGISTER,0B,01,00

REGISTER,0C,01,00

REGISTER,0D,01,00

REGISTER,0E,01,00

REGISTER,0F,01,1E

REGISTER,10,01,1E

REGISTER,11,01,00

REGISTER,12,01,00

REGISTER,13,01,00

REGISTER,14,01,00

REGISTER,15,01,10

//0426

REGISTER,16,01,10

//0426

REGISTER,17,01,03

REGISTER,18,01,03

REGISTER,19,01,00

REGISTER,1A,01,00

REGISTER,1B,01,00

REGISTER,1C,01,00

REGISTER,1D,01,00

REGISTER,1E,01,44

REGISTER,1F,01,80

REGISTER,20,01,02

//CLKA Rise START

REGISTER,21,01,03

//CLKA FALL END

REGISTER,22,01,00

REGISTER,23,01,00

REGISTER,24,01,00

REGISTER,25,01,00

REGISTER,26,01,00

REGISTER,27,01,00

REGISTER,28,01,33

//CLK\_x\_Numb[2:0] Phase\_CLK[2:0]

REGISTER,29,01,03

//Overlap\_CLK[3:0]

REGISTER,2A,01,00  
REGISTER,2B,01,00  
REGISTER,2C,01,00  
REGISTER,2D,01,00  
REGISTER,2E,01,00  
REGISTER,2F,01,00  
REGISTER,30,01,00  
REGISTER,31,01,00  
REGISTER,32,01,00  
REGISTER,33,01,00  
REGISTER,34,01,04  
REGISTER,35,01,00  
REGISTER,36,01,00  
REGISTER,37,01,00  
REGISTER,38,01,3C  
REGISTER,39,01,00  
REGISTER,3A,01,00  
REGISTER,3B,01,00  
REGISTER,3C,01,00  
REGISTER,3D,01,00  
REGISTER,3E,01,00  
REGISTER,3F,01,00  
REGISTER,40,01,00  
REGISTER,41,01,00  
REGISTER,42,01,00  
REGISTER,43,01,00  
REGISTER,44,01,00

//04 GPWR1/2 non overlap time 2.62us

//78 FOR GPWR1/2 cycle 2 s

//GIP\_2

REGISTER,50,01,01  
REGISTER,51,01,23  
REGISTER,52,01,45  
REGISTER,53,01,67  
REGISTER,54,01,89  
REGISTER,55,01,AB  
REGISTER,56,01,01  
REGISTER,57,01,23  
REGISTER,58,01,45  
REGISTER,59,01,67  
REGISTER,5A,01,89  
REGISTER,5B,01,AB  
REGISTER,5C,01,CD  
REGISTER,5D,01,EF

//GIP\_3

REGISTER,5E,01,11  
REGISTER,5F,01,01  
REGISTER,60,01,00  
REGISTER,61,01,15

//GOUT1\_FW  
//GOUT2\_BW  
//GOUT3\_GPWR1

```

REGISTER,62,01,14 //GOUT4_GPWR2
REGISTER,63,01,0C //GOUT5_CLK1_R
REGISTER,64,01,0D //GOUT6_CLK2_R
REGISTER,65,01,0E //GOUT7_CLK3_R
REGISTER,66,01,0F //GOUT8_CLK4_R
REGISTER,67,01,06 //GOUT9_STV1_R
REGISTER,68,01,02
REGISTER,69,01,02
REGISTER,6A,01,02
REGISTER,6B,01,02
REGISTER,6C,01,02
REGISTER,6D,01,02
REGISTER,6E,01,08 //GOUT16_STV2_R
REGISTER,6F,01,02 //GOUT17_VGL
REGISTER,70,01,02 //GOUT18_VGL
REGISTER,71,01,02 //GOUT19_VGL
REGISTER,72,01,02
REGISTER,73,01,02
REGISTER,74,01,02

REGISTER,75,01,01 //FW
REGISTER,76,01,00 //BW
REGISTER,77,01,14 //GPWR1
REGISTER,78,01,15 //GPWR2
REGISTER,79,01,0C //CLK1_R
REGISTER,7A,01,0D //CLK2_R
REGISTER,7B,01,0E //CLK3_R
REGISTER,7C,01,0F //CLK4_R
REGISTER,7D,01,08 //STV1_R
REGISTER,7E,01,02
REGISTER,7F,01,02
REGISTER,80,01,02
REGISTER,81,01,02
REGISTER,82,01,02
REGISTER,83,01,02
REGISTER,84,01,06 //STV2_R
REGISTER,85,01,02 //VGL
REGISTER,86,01,02 //VGL
REGISTER,87,01,02 //VGL
REGISTER,88,01,02
REGISTER,89,01,02
REGISTER,8A,01,02

//CMD_Page 4
REGISTER,FF,03,98,81,04
REGISTER,6C,01,15 //Set VCORE voltage =1.5V
REGISTER,6E,01,2A //di_pwr_reg=0 for power mode 2A //VGH clamp 15V
REGISTER,6F,01,33 // reg vcl + pumping ratio VGH=3x VGL=-2x
REGISTER,3A,01,24 //POWER SAVING
REGISTER,8D,01,14 //-10V //VGL clamp -12V

```

REGISTER,87,01,BA //ESD  
REGISTER,26,01,76  
REGISTER,B2,01,D1  
REGISTER,B5,01,27 //GMA BIAS  
REGISTER,31,01,75 //SRC BIAS  
REGISTER,30,01,03 //SRC OUTPUT BIAS  
REGISTER,3B,01,98 //PUMP SHIFT CLK  
REGISTER,35,01,1f //HZ\_opt 0426  
REGISTER,33,01,14 //Blanking frame 設定為 GND  
REGISTER,7A,01,0F  
REGISTER,38,01,02  
REGISTER,39,01,00

//CMD\_Page 1

REGISTER,FF,03,98,81,01  
REGISTER,22,01,0A //BGR, SS  
REGISTER,31,01,00 //column inversion  
REGISTER,53,01,3E //VCOM1

REGISTER,50,01,E9 //VREG1OUT=5.5V  
REGISTER,51,01,E5 //VREG2OUT=-5.5V  
REGISTER,60,01,19 //SDT=2.5  
REGISTER,63,01,00

REGISTER,A0,01,08 //VP255 Gamma P  
REGISTER,A1,01,10 //VP251  
REGISTER,A2,01,26 //VP247  
REGISTER,A3,01,03 //VP243  
REGISTER,A4,01,25 //VP239  
REGISTER,A5,01,1B //VP231  
REGISTER,A6,01,13 //VP219  
REGISTER,A7,01,1C //VP203  
REGISTER,A8,01,83 //VP175  
REGISTER,A9,01,19 //VP144  
REGISTER,AA,01,24 //VP111  
REGISTER,AB,01,79 //VP80  
REGISTER,AC,01,23 //VP52  
REGISTER,AD,01,1E //VP36  
REGISTER,AE,01,5C //VP24  
REGISTER,AF,01,28 //VP16  
REGISTER,B0,01,29 //VP12  
REGISTER,B1,01,56 //VP8  
REGISTER,B2,01,63 //VP4  
REGISTER,B3,01,39 //VP0

REGISTER,C0,01,08 //VN255 GAMMA N  
REGISTER,C1,01,20 //VN251  
REGISTER,C2,01,26 //VN247  
REGISTER,C3,01,20 //VN243

REGISTER,C4,01,06 //VN239  
REGISTER,C5,01,35 //VN231  
REGISTER,C6,01,27 //VN219  
REGISTER,C7,01,22 //VN203  
REGISTER,C8,01,92 //VN175  
REGISTER,C9,01,20 //VN144  
REGISTER,CA,01,2B //VN111  
REGISTER,CB,01,81 //VN80  
REGISTER,CC,01,1A //VN52  
REGISTER,CD,01,22 //VN36  
REGISTER,CE,01,4E //VN24  
REGISTER,CF,01,26 //VN16  
REGISTER,D0,01,2D //VN12  
REGISTER,D1,01,56 //VN8  
REGISTER,D2,01,63 //VN4  
REGISTER,D3,01,39 //VN0

//CMD\_Page 0

REGISTER,FF,03,98,81,00  
REGISTER,11,00//sleep out  
delay,120  
REGISTER,29,00//display on  
REGISTER,35,00//TE on

WINSTAR DISPLAY Co., Ltd.



**1、Panel Specification :**

- 1. Panel Type :  Pass  NG , \_\_\_\_\_
- 2. View Direction :  Pass  NG , \_\_\_\_\_
- 3. Numbers of Dots :  Pass  NG , \_\_\_\_\_
- 4. View Area :  Pass  NG , \_\_\_\_\_
- 5. Active Area :  Pass  NG , \_\_\_\_\_
- 6. Operating Temperature :  Pass  NG , \_\_\_\_\_
- 7. Storage Temperature :  Pass  NG , \_\_\_\_\_
- 8. Others : \_\_\_\_\_

**2、Mechanical**

- 1. PCB Size :  Pass  NG , \_\_\_\_\_
- 2. Frame Size :  Pass  NG , \_\_\_\_\_
- 3. Material of Frame :  Pass  NG , \_\_\_\_\_
- 4. Connector Position :  Pass  NG , \_\_\_\_\_
- 5. Fix Hole Position :  Pass  NG , \_\_\_\_\_
- 6. Backlight Position :  Pass  NG , \_\_\_\_\_
- 7. Thickness of PCB :  Pass  NG , \_\_\_\_\_
- 8. Height of Frame to PCB :  Pass  NG , \_\_\_\_\_
- 9. Height of Module :  Pass  NG , \_\_\_\_\_
- 10. Others :  Pass  NG , \_\_\_\_\_

**3、Relative Hole Size :**

- 1. Pitch of Connector :  Pass  NG , \_\_\_\_\_
- 2. Hole size of Connector :  Pass  NG , \_\_\_\_\_
- 3. Mounting Hole size :  Pass  NG , \_\_\_\_\_
- 4. Mounting Hole Type :  Pass  NG , \_\_\_\_\_
- 5. Others :  Pass  NG , \_\_\_\_\_

**4、Backlight Specification :**

- 1. B/L Type :  Pass  NG , \_\_\_\_\_
- 2. B/L Color :  Pass  NG , \_\_\_\_\_
- 3. B/L Driving Voltage (Reference for LED Temperature) :  Pass  NG , \_\_\_\_\_
- 4. B/L Driving Current :  Pass  NG , \_\_\_\_\_
- 5. Brightness of B/L :  Pass  NG , \_\_\_\_\_
- 6. B/L Solder Method :  Pass  NG , \_\_\_\_\_
- 7. Others :  Pass  NG , \_\_\_\_\_

>> **Go to page 2** <<



Winstar      Module Number : \_\_\_\_\_

Page: 2

**5、Electronic Characteristics of Module :**

- 1. Input Voltage :                       Pass                       NG , \_\_\_\_\_
- 2. Supply Current :                       Pass                       NG , \_\_\_\_\_
- 3. Driving Voltage for LCD :            Pass                       NG , \_\_\_\_\_
- 4. Contrast for LCD :                     Pass                       NG , \_\_\_\_\_
- 5. B/L Driving Method :                 Pass                       NG , \_\_\_\_\_
- 6. Negative Voltage Output :           Pass                       NG , \_\_\_\_\_
- 7. Interface Function :                  Pass                       NG , \_\_\_\_\_
- 8. LCD Uniformity :                     Pass                       NG , \_\_\_\_\_
- 9. ESD test :                             Pass                       NG , \_\_\_\_\_
- 10. Others :                               Pass                       NG , \_\_\_\_\_

**6、Summary :**

Sales signature : \_\_\_\_\_

Customer Signature : \_\_\_\_\_

Date :      /      /      \_\_\_\_\_

WINSTAR DISPLAY Co., Ltd.