晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM-7201280ETZQW-00H
APPROVED BY	
DATE	

☑ Approved For Specifications
☐ Approved For Specifications & Sample

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2015/8/03	-	New Release	Lawlite

1. PHYSICAL SPECIFICATIONS

Item	Specifications	Remark
LCD size	4.99 inch(Diagonal)	
Driver element	a-Si TFT active matrix	
Display resolution	720 (W) × 3(RGB) x 1280(H) dots	
Pixel Configuration	16.7M	
Pixel pitch	0.08625 (W) x0.08625 (H) mm	
Active area	62.1 (W) x 110.4 (H) mm	
Module size	65.4 (W) x 118.9 (H) × 1.45 (D) mm	
Color arrangement	R.G.B-stripe	
LED Numbers	12 LED	
Weight (g)	TBD	
Driver IC	ILI9881C	

Note 1: Requirements on Environmental Protection: Q/S0002

Note 2: LCM weight tolerance: ± 5%

2. ABSOLUTE MAXIMUM RATINGS

GND=0V, Ta = 25℃

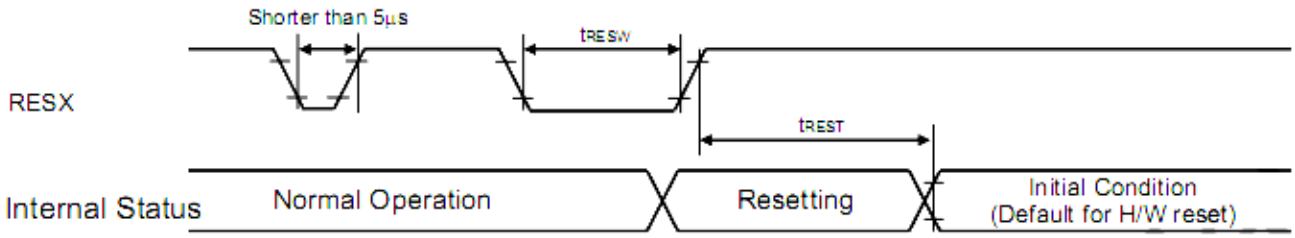
Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	VDDI	-0.3	3.3	V	
Power Supply Voltage	VDD+	-0.3	6.5	V	
	VDD-	0.3	-6.5	V	
Logic Low Level Input voltage	VIL	-0.3	IOVCC*0.3	V	
Logic High Level Input voltage	VIH	IOVCC*0.3	IOVCC		
Back Light Forward Current	I_{LED}	-	25	mA	For Each LED
Operating Temperature	T_{OPR}	-20	70	℃	
Storage Temperature	T_{STG}	-30	80	℃	

3. ELECTRICAL SPECIFICATIONS

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage		IOVCC	1.75	1.8	3.3	V	
Power Supply Voltage		VDD+(VSP)	4.5	5.0	6.0	V	
		VDD-(VSN)	-6.0	-5.0	-4.5		
Input Signal Voltage	Low Level	V_{IL}	GND	--	0.3*VDDI	V	
	High Level	V_{IH}	0.7* VDDI	--	VDDI	V	
Output Signal Voltage	Low Level	V_{OL}	GND	--	0.2* VDDI	V	
	High Level	V_{OH}	0.8* VDDI	--	VDDI	V	

4 Timing Characteristics

4.1 Reset timing characteristics



Reset input timing

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1)Reset low Pulse width	RESX	10	-	-	-	µs
t_{REST}	*2)Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

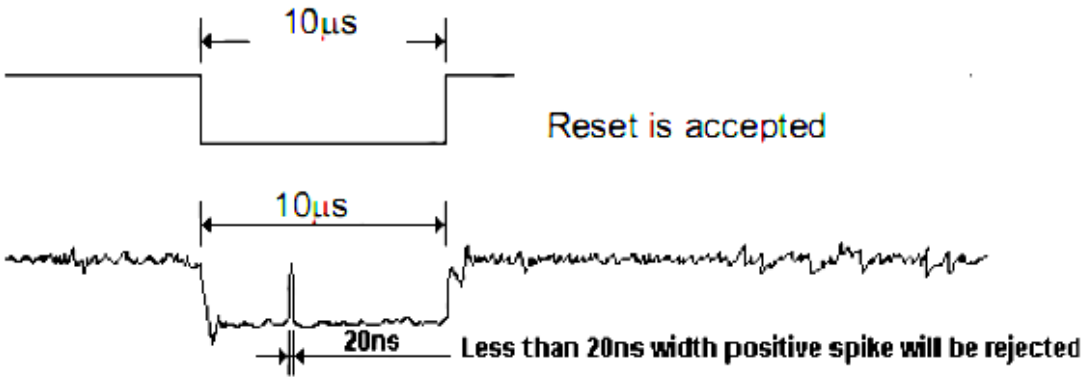
Note 1. Spike due to an electrostatic on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset starts (It depends on voltage and temperature condition)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, ID1/ID2/ID3/ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after arising edge of RESX.

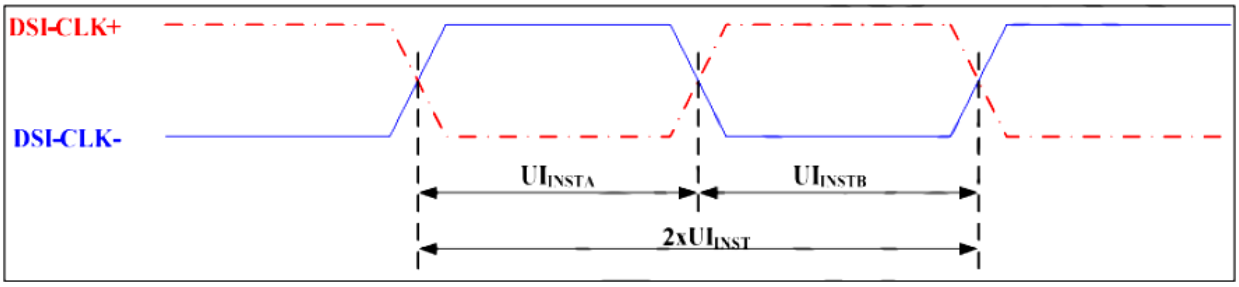
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

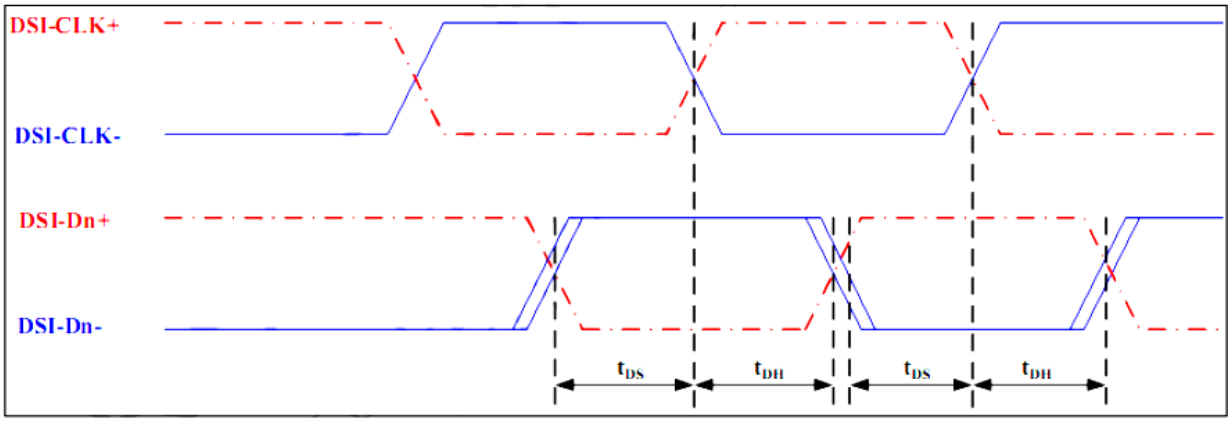


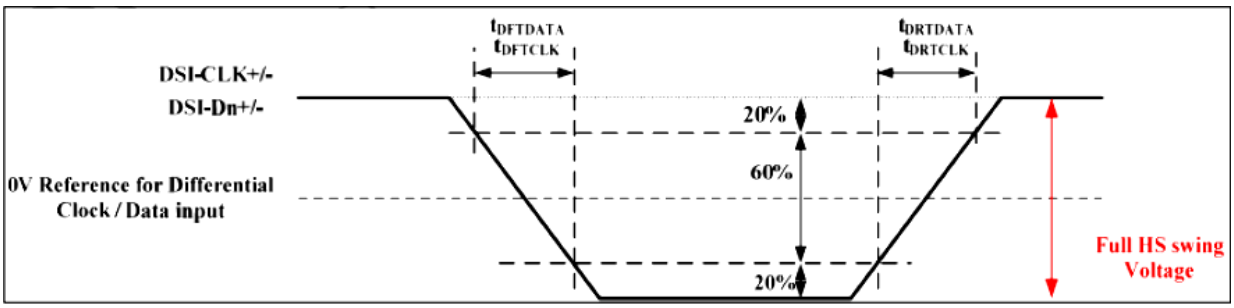
Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

4.2 High Speed Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	-	25	ns
DSI-CLK+/-	UI_{INSTA}, UI_{INSS}	UI instantaneous Halfs	2	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hole time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.31UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.31UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.31UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.31UI	ps



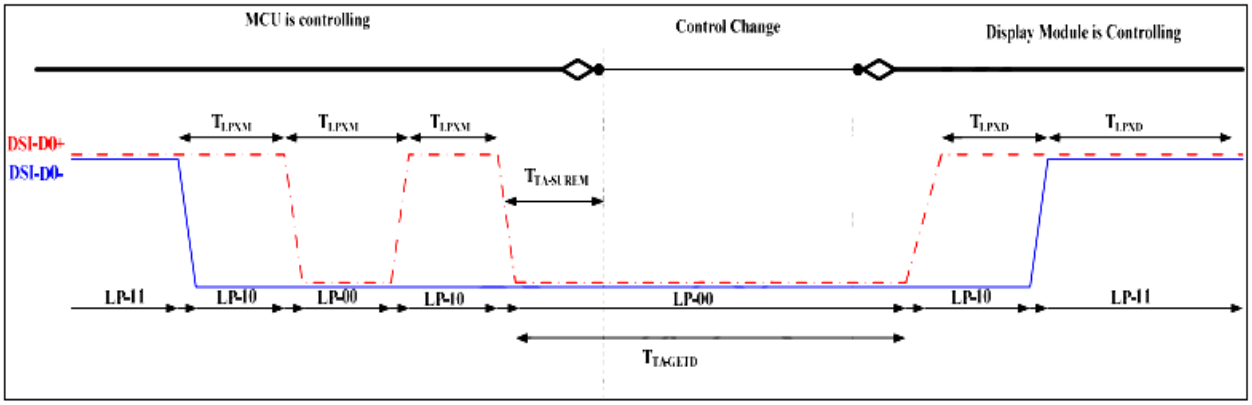




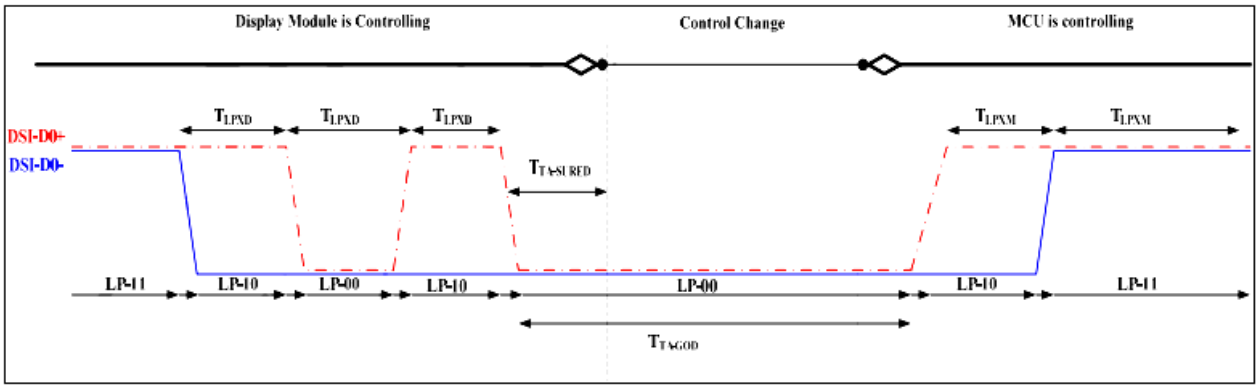
AC characteristics for MIPI-DSI High speed mode

4.3 Low Speed Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU→ Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module→ MPU	58	-	-	ns
DSI-D0+/-	$T_{TA.SURED}$	Time-out before the MPU Start driving	T_{LPXD}	-	2X T_{LPXD}	ns
DSI-D0+/-	$T_{TA.GETD}$	Time to drive LP-00 by Display module	5X T_{LPXD}	-	-	ns
DSI-D0+/-	$T_{TA.GOD}$	Time to drive LP-00 after Turnaround request-MPU	4X T_{LPXD}	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM}/ T_{LPXD} between MCU and display module	2/3	-	3/2	



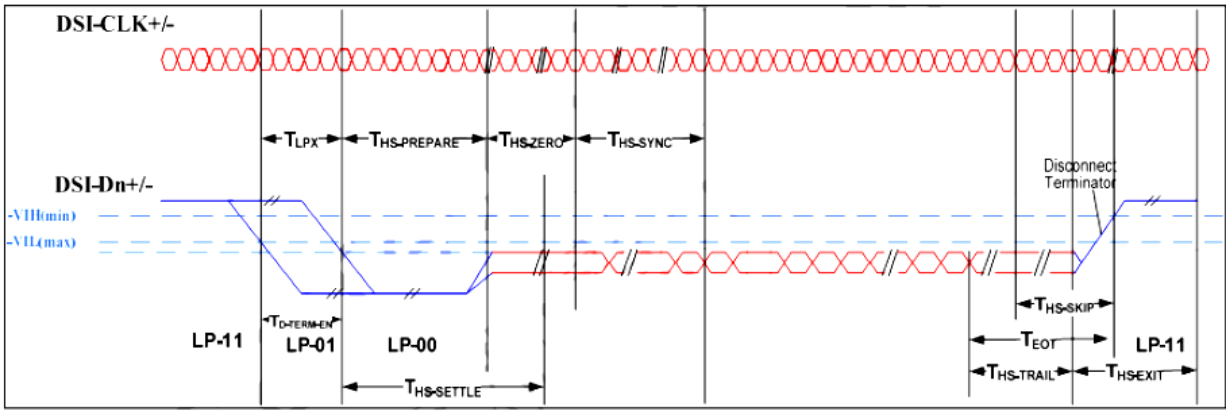
BTA from the MCU to the Display Module



BTA from the Display Module to the MCU

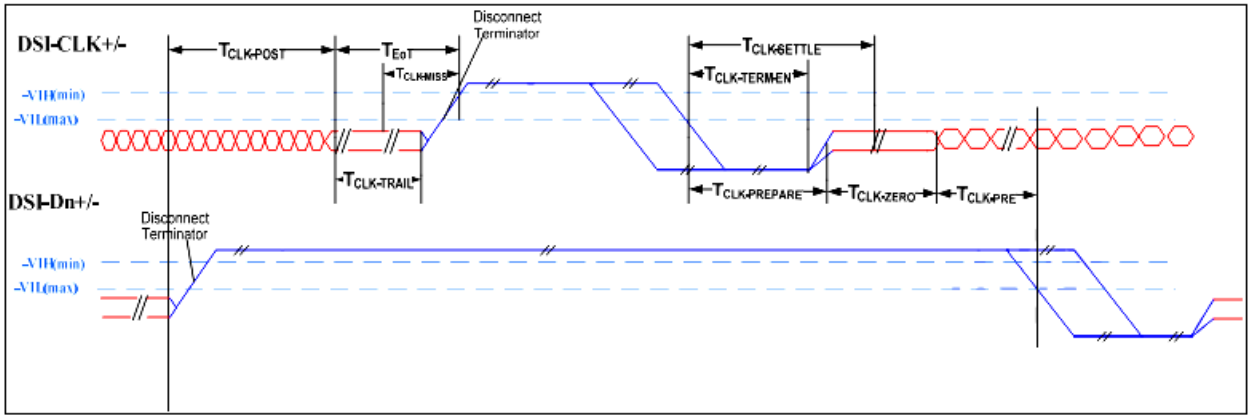
4.4 Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Hight Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS.PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns+ 4UI	-	85ns+ 6UI	ns
DSI-Dn+/-	$T_{HS.PREPARE}$ + $T_{HS.ZERO}$	$T_{HS.PREPARE}$ + time to drive HS-0 before the sync sequence	145ns+ 10UI	-	-	ns
DSI-Dn+/-	$T_{D.TERM.EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM.EN}$	-	35ns+ 4UI	ns
DSI-Dn+/-	$T_{HS.SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+ 4UI	ns
DSI-Dn+/-	$T_{HS.TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max(8UI ,60ns+ 4UI)	-	-	ns
DSI-Dn+/-	$T_{HS.EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105ns +12UI	ns



High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lance between clock Trans mission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns +52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK.PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK.TERM.EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM.EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK.PREPARE}$ +$T_{CLK.ZERO}$	$T_{CLK.PREPARE}$ + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK.TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK.TRAIL}$ period to start of LP-11 state	-	-	105ns +12UI	ns



Switching the clock Lane between clock Transmission and Low Power Mode

4.5 LP-11 between High Speed and Low Power Modes

D SI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when 4 different combinations, what are listed below, are possible:

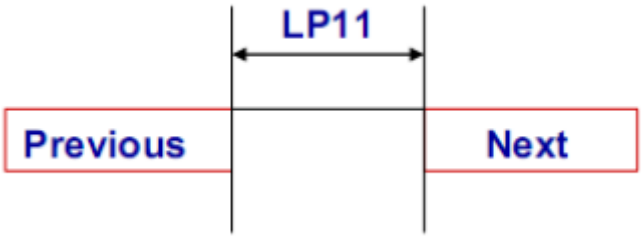
1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Speed Mode
3. Low Speed Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Speed Mode => Stop State (SS, LP-11) => Low Speed Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from previous mode to Next mode

Next / Previous	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100ns	-	100ns	-	100ns	-
HSDT	60ns+ 52UI	-	60ns+ 52UI	-	60ns+ 52UI	-
BTA	100ns	-	100ns	-	100ns	-

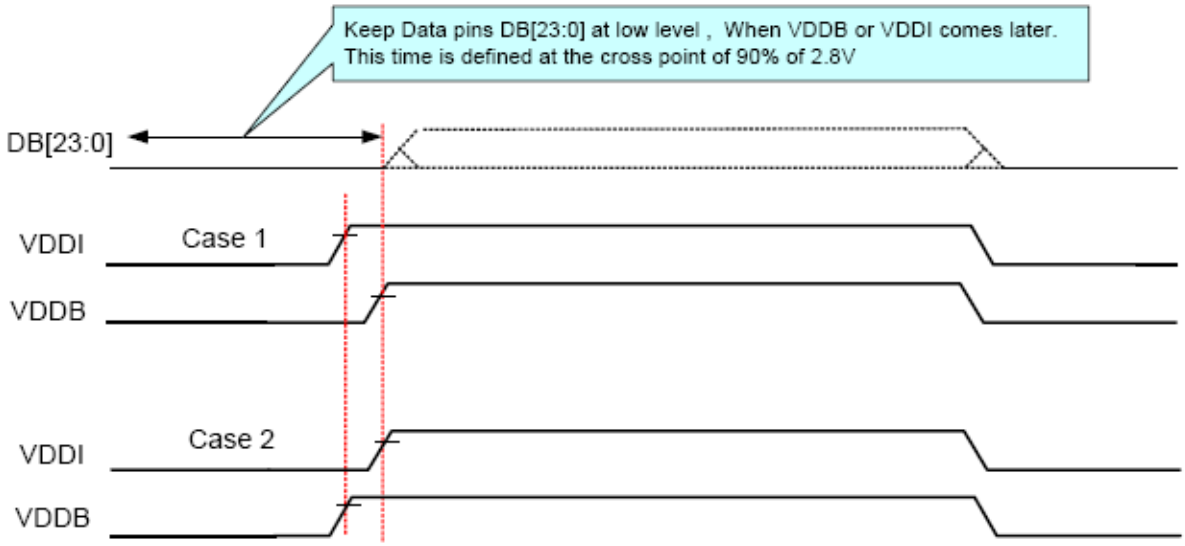


4.6 POWER ON/OFF SEQUENCE

VDDI and VDDA can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note:

1. There will be no damage to ILI19806C if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 13.1 and 13.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. Keep data pins DB[23:0] at low level, when VDDB or VDDI comes later



5 Input/Output Terminals

Pin No.	Symbol	I/O	Function
1	GND	p	Power ground
2	LEDK2	P	Cathode for LED backlighting
3	LEDK1	p	Cathode for LED backlighting
4	LEDA	P	Anode for LED backlighting
5	GND	p	Power ground
6	CABC	P	CABC function enable
7	GND	P	Power ground
8	TE	I/O	
9	ID_GPIO(GND)	I	ID
10	RESET	I	Reset pin
11	ID_ADC	I	ID
12	IOVCC(1.8V)	P	1.8V
13	GND	P	Power ground
14	VDD(+5V)	P	+5V
15	GND	P	Power ground
16	VDD(-5V)	P	-5V
17	GND	P	Power ground
18	OTP	I/O	NC
19	GND	P	Power ground
20	LAN3_P	I	MIPI data input
21	LAN3_N	I	MIPI data input
22	GND	P	Power ground

23	LAN2_P	I	MIPI data input
24	LAN2_N	I	MIPI data input
25	GND	P	Power ground
26	CLK_P	I	MIPI CLK input
27	CLK_N	I	MIPI CLK input
28	GND	P	Power ground
29	LAN1_P	I	MIPI data input
30	LAN1_N	I	MIPI data input
31	GND	P	Power ground
32	LAN0_P	I	MIPI data input
33	LAN0_N	I	MIPI data input
34	GND	P	Power ground

Note1：Please add the FPC connector type and matched one if necessary.

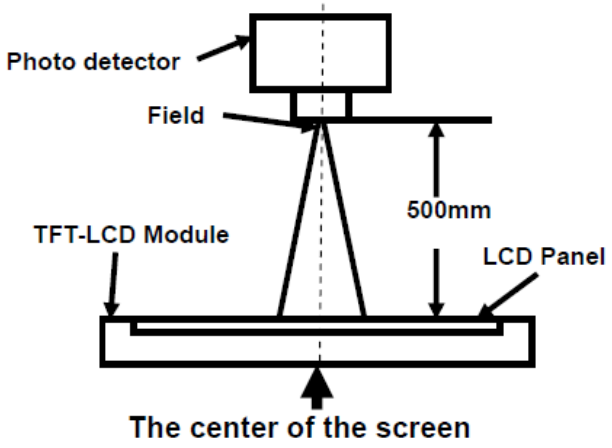
6 Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10		80		Degree	Note2,3
		θB			80			
		θL			80			
		θR			80			
Contrast Ratio		CR	θ=0°	600	800			Note 3
Response Time		T_{ON}	25℃	-	35		ms	Note 4
		T_{OFF}						
Chromaticity	**White**	x	Backlight is on	0.26	0.29	0.32		Note 1,5
		y		0.28	0.30	0.34		
	Red	x		0.571	0.621	0.671		Note 1,5
		y		0.271	0.321	0.371		
	Green	x		0.261	0.311	0.361		Note 1,5
		y		0.579	0.629	0.679		
	Blue	x		0.105	0.155	0.205		Note 1,5
		y		0.002	0.052	0.102		
Uniformity		U		70	80		%	Note 6
NTSC					70		%	Note 5
Luminance		L		400	430		cd/m^2	Note 7

Test Conditions:

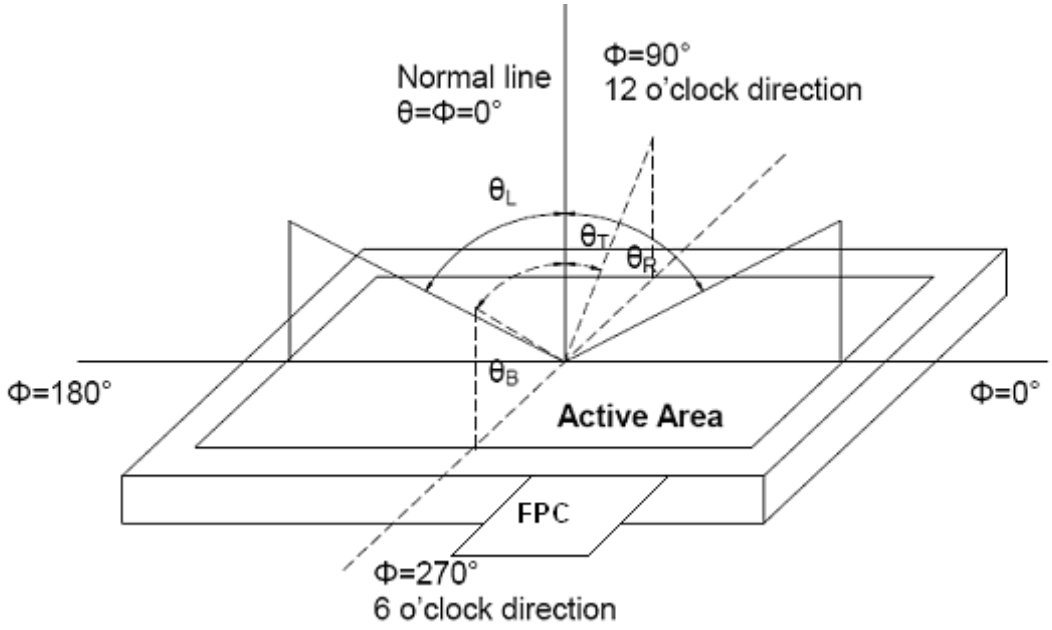
1. I_F= **20**mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical
properties are measured at the center point of the LCD screen. All input terminals LCD panel must
be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。



Note 3: Definition of contrast ratio

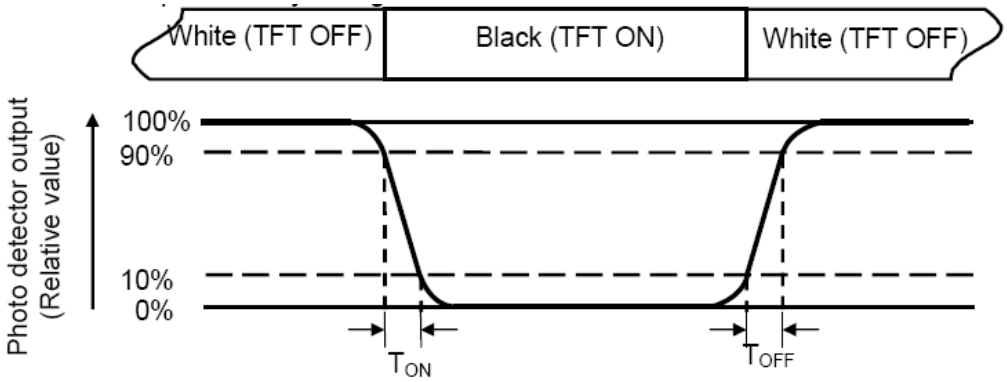
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

“White state “: The state is that the LCD should drive by Vwhite.
“Black state”: The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10%to 90%.



Note 5: Definition of color chromaticity (CIE1931)

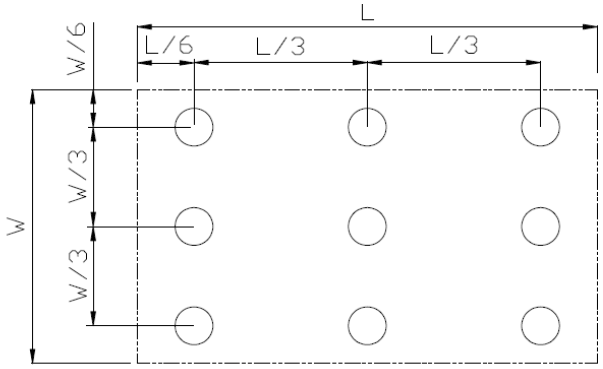
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at avg of 9 point.

7 Environmental / Reliability Test

No	Test Item	Test condition	Remark
1	High Temperature Storage	70℃±2℃96Hrs	
2	Low Temperature Storage	-30℃±2℃ 96Hrs	
3	High Temperature Operation	60℃±2℃96Hrs	
4	Low Temperature Operation	-20℃±2℃ 96Hrs	
5	High Temperature & Humidity Storage	60℃±2℃ 90%RH 96Hrs	
6	Temperature Cycle	-30℃ →70℃ 30min 30min after 32cycle, change time 30s Restore 2H at 25℃ Power off	
7	Vibration Test	Frequency:10Hz~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz, 120min ±x,±Y,±Z for each direction	1Carton-box
8	Shock Test	Half-sine wave,600m/s2,6ms ±x,±Y,±Z 3 times,for each direction	-
9	Drop Test(package state)	800mm, concrete floor,1corner, 3edges, 6 sides each time	1Carton-box
10	ESD Sensitivity test	5points/panel Contact ±4KV，150PF/330，5times Air ±8KV,150PF/330，5times	-

NOTE:

1.Sample size for each test item is 5~10pcs.

2.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

3.In case of malfunction defect caused by ESD damage, if it would be recovered to normal

state after resetting, it would be judge as a good part. Using ionizer(an antistatic blower)

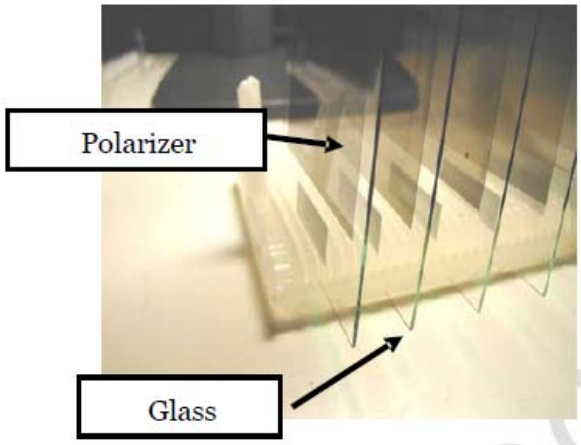
is recommended at working area in order to reduce electro-static voltage. When removing protection film from LCM panel, peel off the tag slowly(recommended more than one second) while blowing with ionizer toward the peeling face to minimize ESD which may damage electrical circuit.

4. EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.

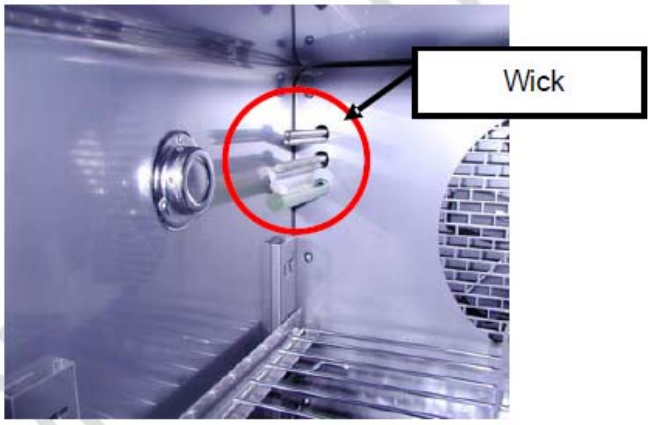
5. Polarizer test criteria

a. when testing avoid samples take out then return, It can cause water coagulation in Polarizer. Increase the distance of samples , And put samples before the wind.

b. When the samples are put into the test, put them upright so that the glasses keep spaces between them each other. (Picture 9.1)



Picture 9.1



Picture 9.2

c. Put samples into testing machine as small as possible so that it is drafty.

d. Do not put samples under wick because water will fall.(Picture 9.2)

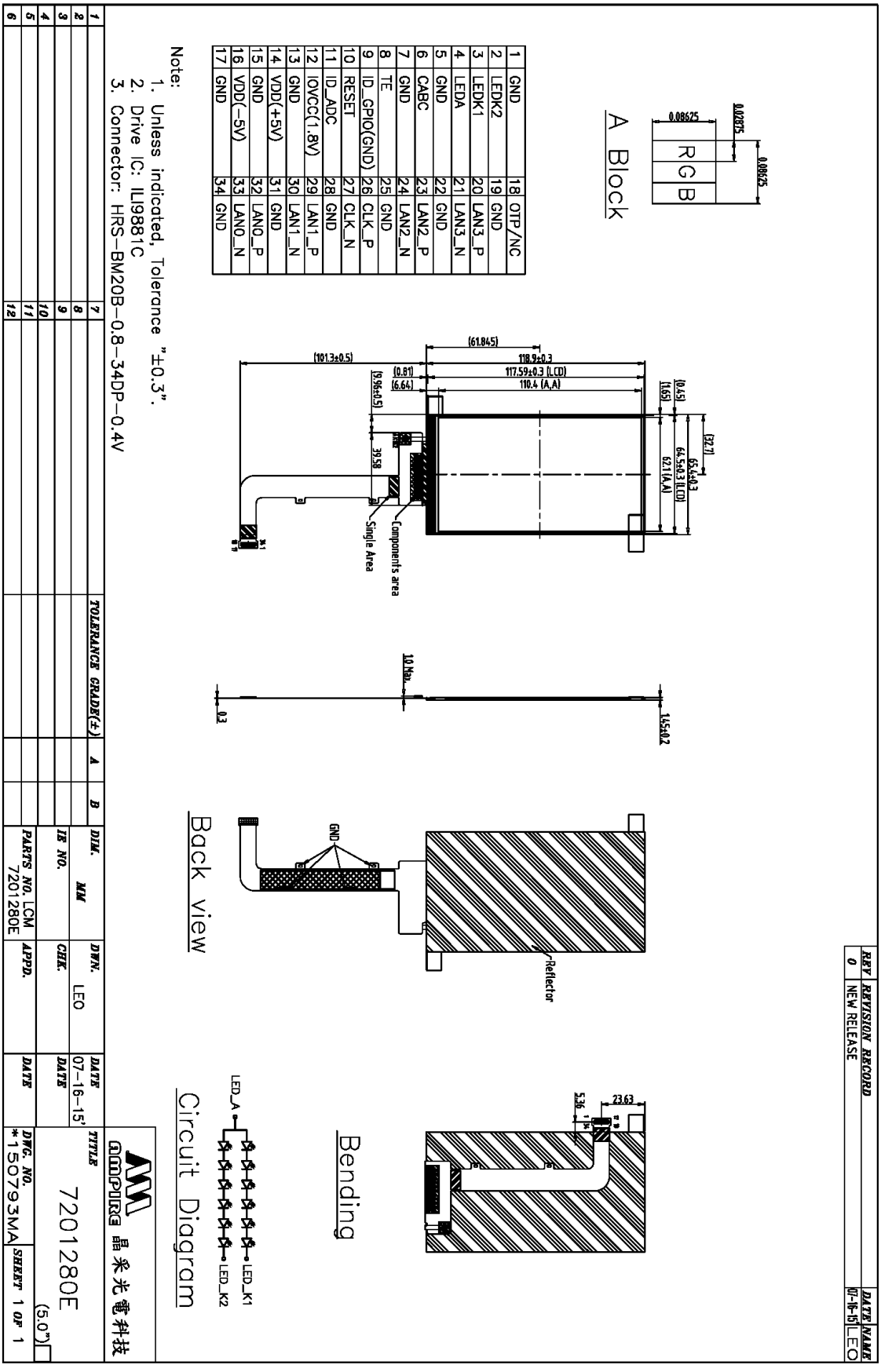
e. Do not open testing machine except for taking them out in order to prevent moisture condensation.

6. Please use automatic switch menu(or roll menu) testing mode when test operating mode

7. The inspection terms after reliability test, as below

ITEM	Inspection standard
Contrast	CR>50%
IDD	IDD<200%
Brightness	Brightness>60%
Color Tone	Color Tone+/-0.05

8. OUTLINE DIMENSION



1	GND	18	OTP/NC
2	LEDK2	19	GND
3	LEDK1	20	LAN3_P
4	LEDA	21	LAN3_N
5	GND	22	GND
6	CABC	23	LAN2_P
7	GND	24	LAN2_N
8	TE	25	GND
9	ID_GPIO(GND)	26	CLK_P
10	RESET	27	CLK_N
11	ID_ADC	28	GND
12	IOVCC(1.8V)	29	LAN1_P
13	GND	30	LAN1_N
14	VDD(+5V)	31	GND
15	GND	32	LAN0_P
16	VDD(-5V)	33	LAN0_N
17	GND	34	GND