晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO	**AM-480272M3TNQW-C2H**
APPROVED BY	
DATE	

☐ **Approved For Specifications**
☐ **Approved For Specifications & Sample**

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RECORD   OF   REVISION

Revision Date	Page	Contents	Editor
2012/3/23	-	New Release	Patrick
2013/06/19	-	Correct mechanical drawing. Correct the Part No to AM-480272M3TNQW-C2H	Bob

1. FEATURES

    (1)   Construction : a-Si TFT-LCD with driving system, White LED Backlight

    (2)   LCD type : Transmissive , Normally White

    (3)   LCD Controller FSA506, i80/16Bit MPU interface

    (4)   Built in LED driver

2. PHYSICAL SPECIFICATIONS

Item	Specifications	unit
Display size (diagonal)	4.3	inch
Resolution	480RGB (W) x 272(H)	dots
Display area	95.04(W) x 53.86 (H)	mm
Pixel pitch	0.198 (W) x 0.198 (H)	mm
Overall dimension	105.5(W) x 67.2(H) x 5.71(D)	mm
Color configuration	R.G.B Vertical stripe	
Viewing Direction (Gray Inversion)	12 o'clock	

3. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit
Operation Temperature	T_{OP}	-20	70	℃
Storage Temperature	T_{ST}	-30	80	℃

4. OPTICAL CHARACTERISTICS

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	60	70	--	Degree	Note 2
		θB		40	50	--		
		θL		60	70	--		
		θR		60	70	--		
Contrast Ratio		CR	θ=0°	400	500	--		Note1、Note3
Response Time		T$_{ON}$	25℃	--	20	30	ms	Note1 Note4
		T$_{OFF}$						
Chromaticity	White	x	Backlight is on	0.265	0.315	0.365		Note5 Note1
		y		0.285	0.335	0.385		
	Red	x		0.531	0.581	0.631		
		y		0.295	0.345	0.395		
	Green	x		0.298	0.348	0.395		
		y		0.531	0.581	0.631		
	Blue	x		0.103	0.153	0.203		
		y		0.045	0.095	0.145		
Uniformity		U		75	80	--	%	Note1、Note6
NTSC				--	50	--	%	Note 5
Luminance		L		250	300	--	cd/m^2	Note1、Note7

Test Conditions:
1. I$_F$= 20mA(one channel),the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.
　　　The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.
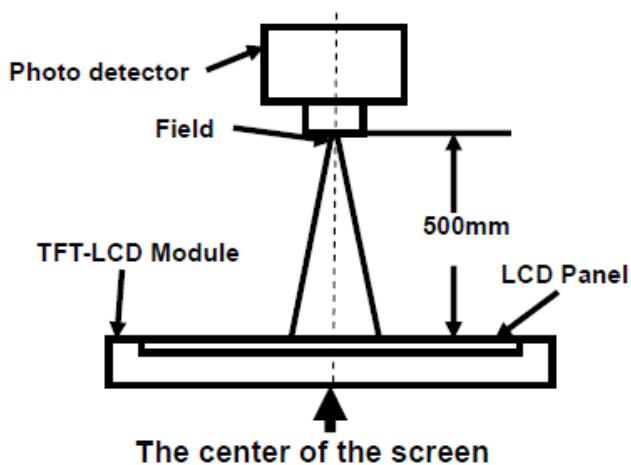
Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system. Viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。
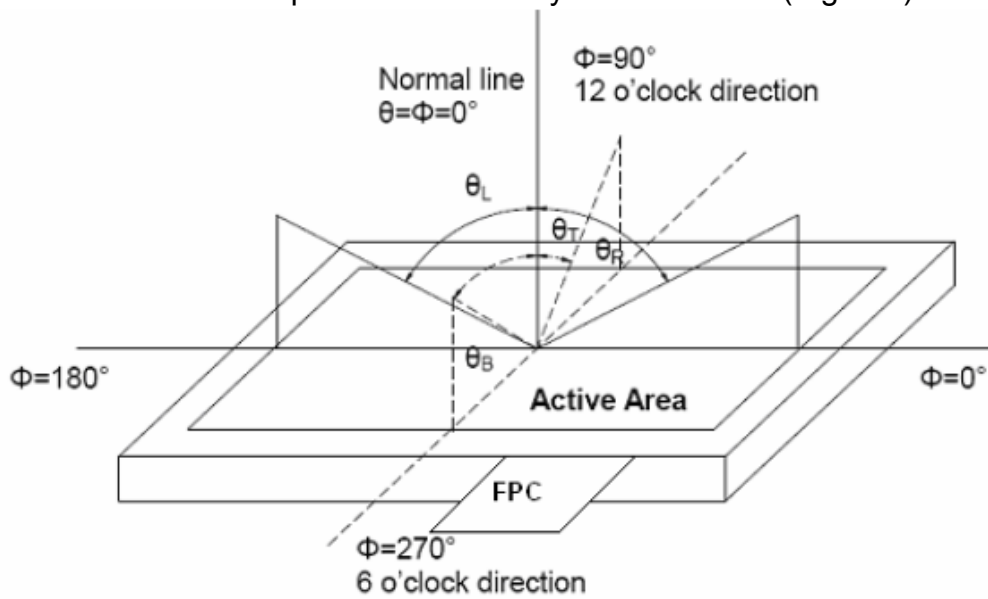

Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

Note 4: Definition of Response time
The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.
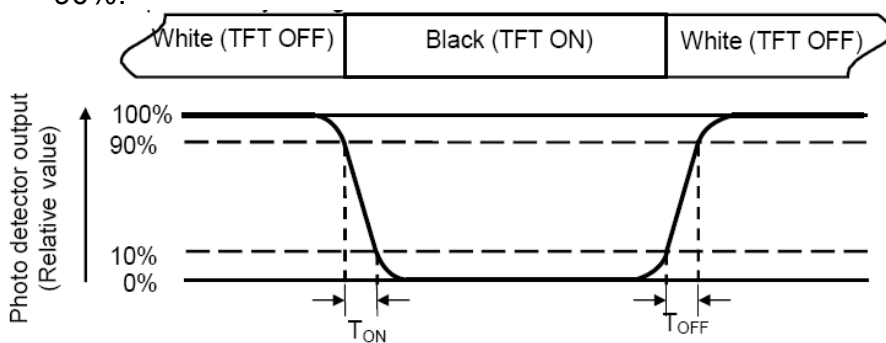
Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity
   Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is
   placed at the center of each measuring area.
   Luminance Uniformity (U) = Lmin/ Lmax
   L-------Active area length W----- Active area width
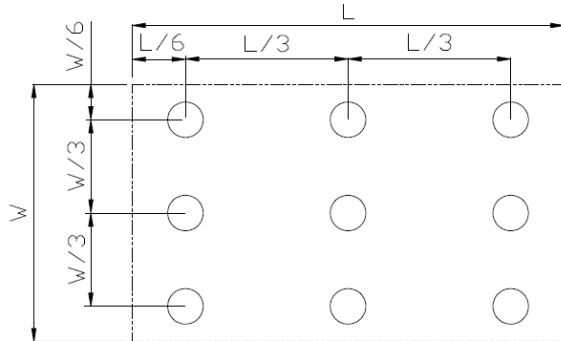
   Lmax: The measured Maximum luminance of all measurement position.
   Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:
   Measure the luminance of white state at center point.

5. ELECTRICAL CHARACTERISTICS

LCD driving

| Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	5.0	V	
Input Voltage for logic	H Level	V_{IH}	2.0	-	5.5	V	Note 1
	L Level	V_{IL}	VSS	-	0.8	V	
Output Voltage for Logic	H Level	V_{OH}	2.4	-	VDD	V	Note 2
	L Level	V_{OL}	VSS		0.4	V	

Note1: With 5V Tolerance Input, /CS, /WR, /RD, RS, DB0~DB17
Note2: DB0~DB17

LED back light

Paramenter	Symbol	Min.	Typ.	Max.	Unit	Condition
LED voltage	VLED	--	16	--	V	I_{LED}=40mA,Ta=25℃
LED forward current	I_{LED}	--	40	-	mA	Ta=25℃
	I_{LED}	--	30	-	mA	Ta=60℃
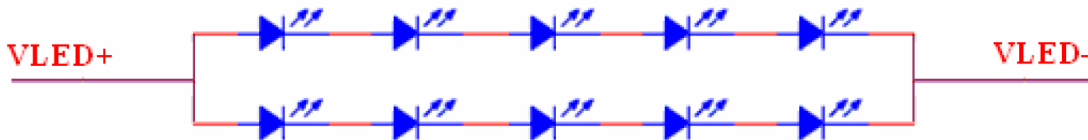
* The built-in LED driver is powered by VDD

* The PWM pin combined enable and brightness adjust function.
  When PWM=High constantly, the LED back-light is turn on.
  When PWM=GND constantly, the LED back-light is turn off.
  When PWM signal (100Hz to 1KHz) input, the LED Back-light brightness is relative to duty cycle of the PWM signal.

6. BLOCK DIAGRAM

480 X RGB X 272

Line 1

Line 272

S1

S1440

Source Driver + T-con

Gate Driver

TFT Panel

PCB circuit

VS HS DE DC LK R6 G6 B6

Output control

VCOM circuit

SRAM 640X240X3X6 bits

PLL

SRAM control

OSC

Power circuit

Input control

TFT LCD controller

LED Driver

LED Backlight

VDD
VSS
/WR (E)
/RD(R/W)
/CS
RS
/RESET
65K/262K
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
DB12
DB13
DB14
DB15
FB16
DB17
NC
NC
NC
NC
NC
LED_A
LED_K

7. INTERFACE

Pin no	Symbol	I/O	Description		Remark
1 ~ 2	VSS		GND		
3	LED_A/PWM		Without LED driver	LED Anode	
			With LED Driver	**PWM**	**Default**
4	LED_K		Without LED driver	LED Cathode	
			With LED Driver	**Must be OPEN**	**Default**
5	/RESET	I	Reset signal for TFT LCD controller		
6	RS	I	Register and Data select for TFT LCD controller		
7	/CS	I	Chip select low active signal for TFT LCD controller		
8	/WR(E)	I	80mode : /WR low active signal for TFT LCD controller 68mode : E signal latch on rising edge		
9	/RD(R/W)	I	80mode : /RD low active signal for TFT LCD controller 68mode : R/W signal Hi: read Lo:Write		
10 ~ 27	DB0 ~ DB17	I/O	Data Bus		
28	65K/262K	I	Select colors data format H : 262K L : 65K		
29	VSS		GND		
30	NC		No connection		
31	NC		No connection		
32	NC		No connection		
33	NC		No connection		
34	NC		No connection		
35 ~ 37	VDD		Power supply for the logic (3.3V)		
38 ~ 40	VSS		GND		

8. INPUT SIGNAL TIMING
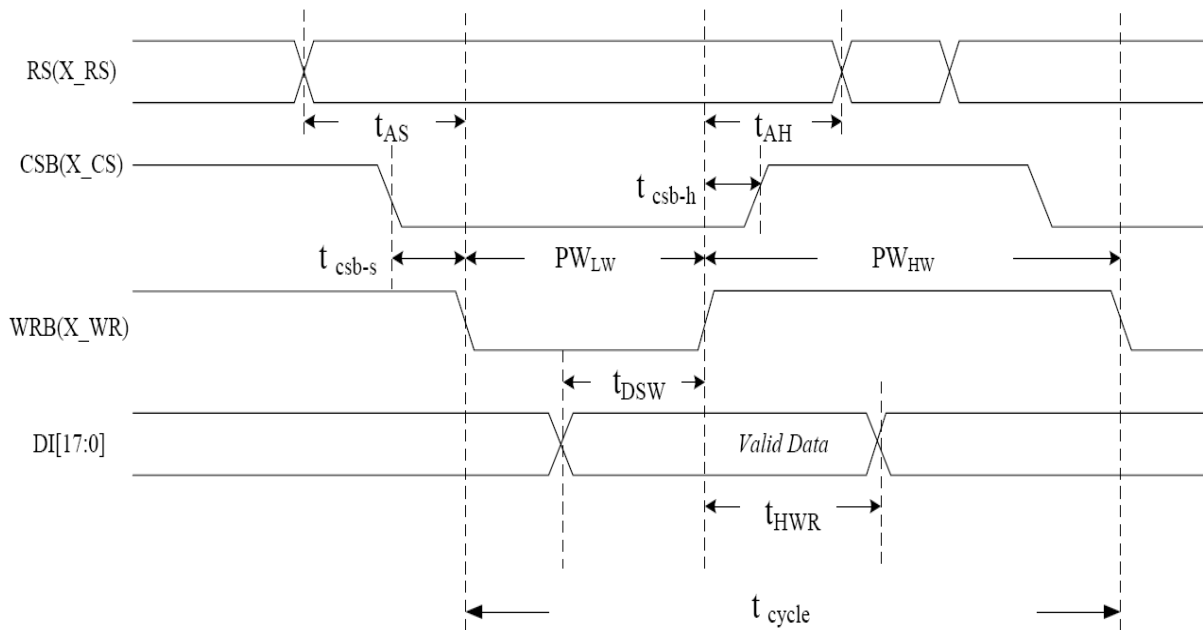
Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{cycle}	Enable cycle time	100	200		ns	
PW_{HW}	Enable high-level pulse width	66	70		ns	
PW_{LW}	Enable low-level pulse width	33	130		ns	
t_{AS}	RS setup time	16	25		ns	
t_{AH}	RS hold time	16	45		ns	
t_{DSW}	Write data setup time	50	50		ns	
t_{HWR}	Write data hold time	40	50		ns	
t_{csb-s}	CSB setup time	16	20		ns	
t_{csb-h}	CSB hold time	16	30		ns	

9 INTERFACE PROTOCOL

16Bit-80/68- Write to Command Register

Note1: DB[7:0] represent the the Register address Addr. DB[15:8] must be 0x00

Note2: DB[7:0] represent the the setting value of the Addr. DB[15:8] must be 0x00

Note3: DB[7:0] represent the the setting value of the Addr+1. DB[15:8] must be 0x00

Note4: DB[7:0] represent the the setting value of the Addr+N. DB[15:8] must be 0x00

Note5: DB[7:0] send 0x80 to Disable the Register write. DB[15:8] must be 0x00
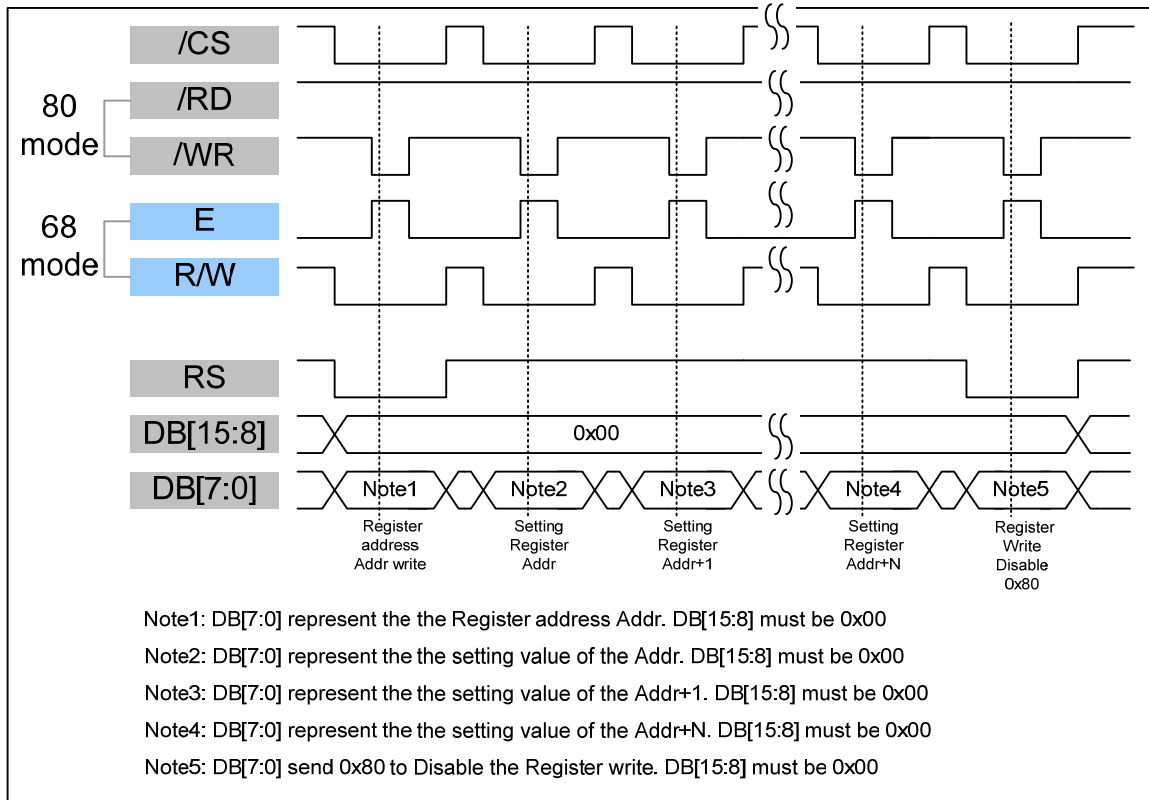
16Bit-80/68-Write to Display RAM

Note1: DB[15:0] send 0x000C1 to Enable the Display RAM write.

Note2: DB[15:0] represent the writing Data1 to Display RAM

Note3: DB[15:0] represent the writing Data2 to Display RAM

Note4: DB[15:0] represent the writing DataN to Display RAM

Note5: DB[15:0] send 0x00080 to Disable the Display RAM write.
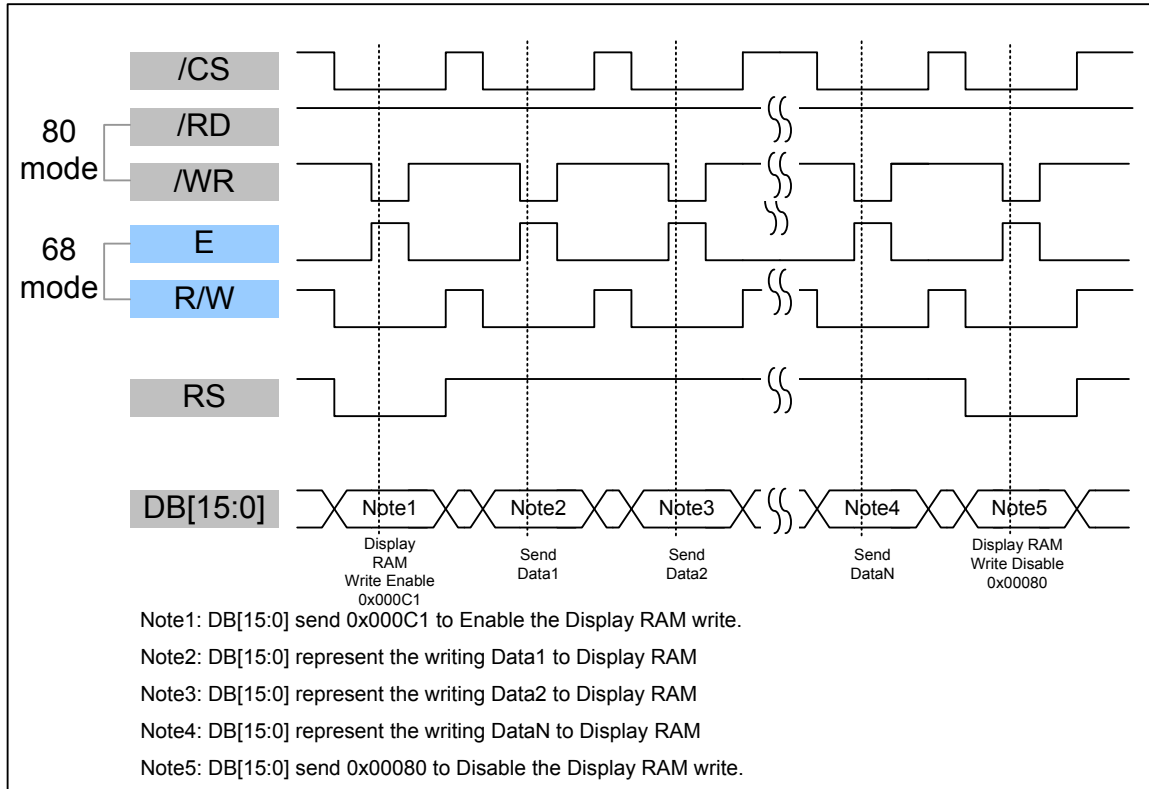
9.1 Data transfer order Setting

16 bit interface 65K color (Pin28 65K/262K =Low)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

16 bit interface 262K color (Pin28 65K/262K =High)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	X	X	X	X	X	X	X	R5	R4
2nd data	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

9.2 Register Depiction

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
00	00	MSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
01	00	LSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
02	01	MSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
03	3F	LSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
04	00	MSB of Y-axis start position								
Description	set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
05	00	LSB of Y-axis start position								
Description	Set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
06	00	MSB of Y-axis end position								
Description	set the vertical end position of display active region									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
07	EF	LSB of Y-axis end position								
Description	Set the vertical end position of display active region									

To simplify the address control of display RAM access, the window area address function allows for writing data only within a window area of display RAM specified by registers REG[00]~REG[07] .

After writing data to the display RAM, the Address counter will be increased within setting window address-range which is specified by
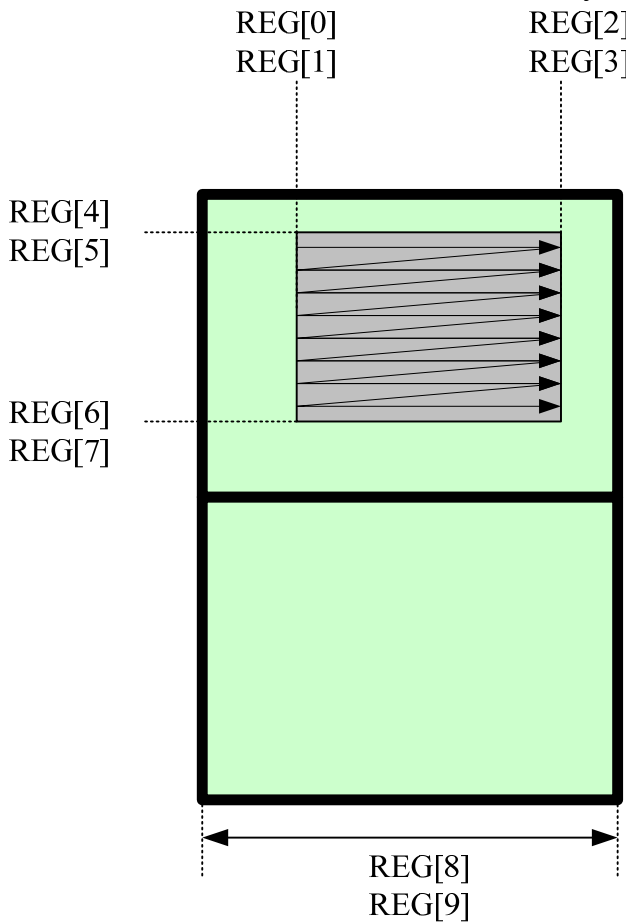
MIN X address (REG[0] & REG[1])

MAX X address (REG[2] & REG[3])

MIN Y address (REG[4] & REG[5])

MAX Y address (REG[6] & REG[7])

Therefore, data can be written consecutively without thinking the data address.

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
08	01	X	X	X	X	X	X	_PanelXSize H_Byte[1:0]		
Description	Set the panel X size									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark

09	40	_PanelXSize L_Byte[7:0]	
Description	Set the panel X size		

The register REG[08] and REG[09] is use to calculate the RAM address. If you want to use the TFT as Landscape mode (320x240), the REG[08] & RGE[09] must set to 320. If you want to use the TFT as Portrait mode (240x320), the REG[08] & RGE[09] must set to 240.

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0A	00	X	X	X	X	X	[17:16] bits of memory write start address			
Description	Memory write start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0B	00	[15:8] bits of memory write start address								
Description	Memory write start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0C	00	[7:0] bits of memory write start address								
Description	Memory write start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x10	0x0D	Bit_SWAP	OUT_TEST	BUS_SEL		Blanking	P/S_SEL	CLK_SEL		
Description	"0x10_Clk_sel[1:0]" : The TFT controller built-in 40Mhz PLL clock. These bits are for select the TFT panel dot clock frequency. 00 : 20Mhz 01: 10Mhz 02: 5 Mhz									
	"0x10_ps_sel[2]" : The TFT controller support parallel and serial RGB interface. These bits are for select the output timing. 0 : serial Panel 1: Parallel panel									
	"0x10_blanking_tmp[3]" 0 : OFF (blanking) 1: ON (normal operation)									
	"0x10_bus_sel[5:4]" : It only for serial Panel 00=R , 01=G , 10=B									
	"0x10_out_test[6]" : Self test 0 : normal operation 1: for test (don't use for normal operation) When set the bit to "1" , the Rout=(Reg 2a[6:0]) Gout=(Reg 2b[6:0]) Bout=(Reg 2c[6:0])									
	"0x10_bit_swap[7]" : 0-normal									
	The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark

0x11	00	X	X	EVEN		_ODD	

Description	" Even line of serial panel data out sequence or data bus order of parallel panel 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved Odd line of serial panel data out sequence 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG **101: BGR** Others: reserved **Must Set to 0x05 for AM320240N1**

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x12	00					Hsync_stH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x13	00				Hsync_stL_Byte[7:0]					
Description	For TFT output timing adjust: Hsync start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x14	00					Hsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x15	10				Hsync_pwL_Byte[7:0]					
Description	For TFT output timing adjust: Hsync pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x16	00					Hact_stH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x17	38				Hact_stL_Byte[7:0]					
Description	For TFT output timing adjust: DE pulse start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x18	01					Hact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x19	40				Hact_pwL_Byte[7:0]					
Description	For TFT output timing adjust: DE pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1A	01					HtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync total clocks H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1B	B8				HtotalL_Byte[7:0]					
Description	For TFT output timing adjust: Hsync total clocks H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1C	00					Vsync_stH_Byte[3:0]				

Description	For TFT output timing adjust: Vsync start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1D	00	Vsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1E	00					Vsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1F	08	Vsync_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x20	00					Vact_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical DE pulse start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x21	12	Vact_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical DE pulse start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x22	00					Vact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical Active width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x23	F0	Vact_pwL_Byte[7:0]								

Description	For TFT output timing adjust: Vertical Active width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x24	01					VtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical total width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x25	09			VtotalL_Byte[7:0]						
Description	For TFT output timing adjust: Vertical total width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
26	00	X	X	X	X	X	[17:16] bits of memory read start address			
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
27	00	[15:8] bits of memory write start address								
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
28	00	[7:0] bits of memory write start address								
Description	Memory read start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
29	00	[7:1] Reversed								
Description	[0] Load output timing related setting (H sync., V sync. and DE) to take effect									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2A	00	X	TestPatternRout[6:0]							

| Description | When " REG[0x10]_out_test[6]" : Self test =1 ;
The Rout data equal to TestPatternRout[6:0] | | | | | | | | | |

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2B	00	X	TestPatternGout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Gout data equal to TestPatternGout[6:0]									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2C	00	X	TestPatternBout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Bout data equal to TestPatternBout[6:0]									

If you set the " REG[0x10]_out_test[6]" : Self test =1 , the TFT controller will skip the connect of the display RAM. The Output port will send the REG[2A] ,REG[2B],REG[2C] data.

REG[2A]=0x3F
REG[2B]=0x00
REG[2C]=0x00

REG[2A]=0x00
REG[2B]=0x3F
REG[2C]=0x00

REG[2A]=0x00
REG[2B]=0x00
REG[2C]=0x3F

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2D	00	X	X	X	X	[3]	Rising/falling edge[2]	_rotate [1:0]		
Description	[3] Output pin X_DCON level control ; TFT Power ON/OFF control 0: TFT POWER circuit OFF 1: TFT POWER circuit ON									
	Rising/falling edge[2] : 0: The RGB out put data are on the Rising edge of the DCLK. 1: The RGB out put data are on the Falling edge of the DCLK.									
	_rotate [1:0]: 00 : rotate 0 degree 01 : rotate90 degree 10 : rotate 270 degree 11 : rotate 180 degree									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
30	00	X	X	X	X	X	_H byte H-Offset[3:0]			
Description	Set the Horizontal offset									
Register	Default	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark

Address (Hex)	(Hex)									
31	00				_L byte H-Offset[7:0]					
Description	Set the Horizontal offset									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
32	00	X	X	X	X	X	_H byte V-Offset[3:0]			
Description	Set the Vertical offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
33	00				_L byte V-Offset[7:0]					
Description	Set the Vertical offset									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
34	00	[7:4] Reserved				_H byte H-def[3:0]				
Description	[3:0] MSB of image horizontal physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
35	40				_L byte H-def[7:0]					
Description	[7:0] LSB of image horizontal physical resolution in memory									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
36	01	[7:4] Reserved				_H byte V-def[3:0]				
Description	[3:0] MSB of image vertical physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
37	E0				_L byte V-def[7:0]					
Description	[7:0] LSB of image vertical physical resolution in memory									

The total RAM size is 640x240x18bit. The user can arrange the Horizontal ram size by REG[34],REG[35] and the Vertical ram size by REG[36],REG[37].
EX: 320x480x18bit REG[34]=0x01 , REG[35]=0x40 , REG[36]=0x01 , REG[37]=0xE0
EX: 640x240x18bit. REG[34]=0x02 , REG[35]=0x80 , REG[36]=0x00 , REG[37]=0xF0

DISPLAYED COLOR AND INPUT DATA

	Color & Gray Scale	DATA SIGNAL																
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(31)	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(61)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(31)	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(1)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(31)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

10. Reliability Test

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 m in. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Humidity Test	40 °C, Humidity 90%, 96 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.
Note 2 : The module should be inspected after 1 hour storage in normal conditions
(15-35°C , 45-65%RH).
Definitions of life end point :
- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11. USE PRECAUTIONS

11.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzene and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

11.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
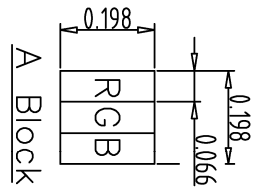3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.

2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.

3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.

4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.

5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.

6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.

7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.
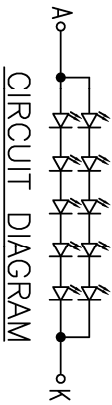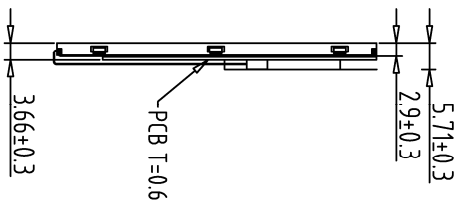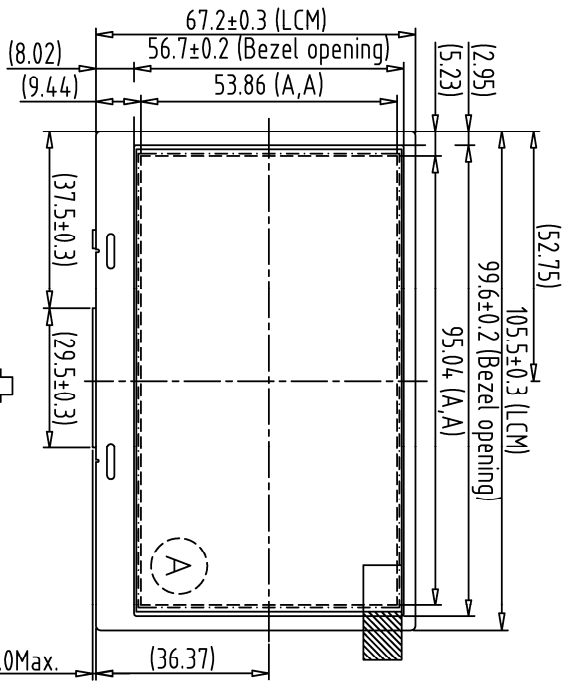
11.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.

2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

12 OUTLINE DIMENSION

A Block

0.198 | 0.198 | 0.066

RGB

Pin assignment table:

1	VSS	21	DB11
2	VSS	22	DB12
3	LED_A	23	DB13
4	LED_A	24	DB14
5	/RESET	25	DB15
6	RS	26	DB16
7	/CS	27	DB17
8	/WR	28	65K
9	/RD	29	VSS
10	DB0	30	NC
11	DB1	31	NC
12	DB2	32	NC
13	DB3	33	NC
14	DB4	34	NC
15	DB5	35	VDD
16	DB6	36	VDD
17	DB7	37	VDD
18	DB8	38	VSS
19	DB9	39	VSS
20	DB10	40	VSS
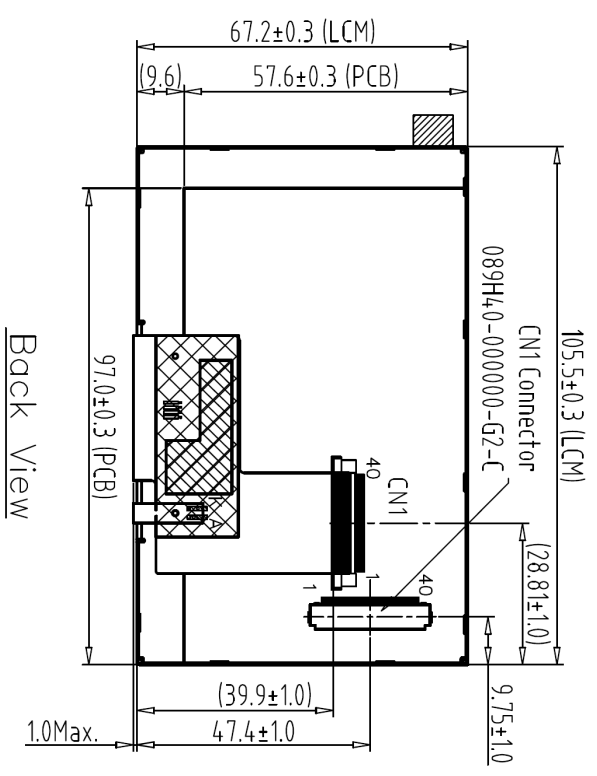
Note:
1. Unless indicated, Tolerance "±0.2"
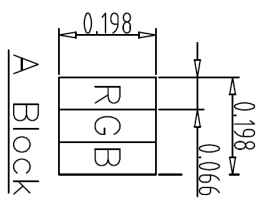2. UV Glue For OLB Protection.
3. Driver IC: HX8257A

CIRCUIT DIAGRAM

Ao —————— oK

Gray Scale Inversion Direction

Dimensions:
- 67.2±0.3 (LCM)
- 56.7±0.2 (Bezel opening)
- 53.86 (A,A)
- (8.02)
- (9.44)
- (2.95)
- (5.23)
- (52.75)
- 105.5±0.3 (LCM)
- 99.6±0.2 (Bezel opening)
- 95.04 (A,A)
- (37.5±0.3)
- (29.5±0.3)
- 1.0Max.
- (36.37)
- 3.66±0.3
- 2.9±0.3
- 5.71±0.3
- PCB T=0.6

TOLERANCE GRADE(±)	A	B
DIM.		
MM		

PARTS NO. LCM
480272M3-C2

DWN.	CHK.	APPD.
Henry		

DATE	DATE	DATE
03-21-12'		

TITLE
480272M3-C2
(4.3")

DWG. NO.
*120374-MB   SHEET 1 OF 1

AMPIRE 晶采光電科技

A Block

RGB		

0.198

0.198

0.066

1	VSS	21	DB11
2	VSS	22	DB12
3	LED_A	23	DB13
4	LED_K	24	DB14
5	/RESET	25	DB15
6	RS	26	DB16
7	/CS	27	DB17
8	/WR	28	65K
9	/RD	29	VSS
10	DB0	30	NC
11	DB1	31	NC
12	DB2	32	NC
13	DB3	33	NC
14	DB4	34	NC
15	DB5	35	NC
16	DB6	36	VDD
17	DB7	37	VDD
18	DB8	38	VSS
19	DB9	39	VSS
20	DB10	40	VSS

Note:
1. Unless indicated, Tolerance "±0.2"
2. UV Glue For OLB Protection.
3. Driver IC: HX8257A

Back View

67.2±0.3 (LCM)

(9.6) 57.6±0.3 (PCB)

105.5±0.3 (LCM)

CN1 Connector
089H40-000000-G2-C

97.0±0.3 (PCB)

CN1

40

1

40

(28.81±1.0)

9.75±1.0

(39.9±1.0)

1.0Max. 47.4±1.0

			TOLERANCE GRADE(±)	A	B	DIM.
1		7				
2		8				IE NO.
3		9				MM
4		10				
5		11				
6		12				

PARTS NO.	LCM-1
480272M3-C2	

DWN. Henry   DATE 03-21-12'
CHK.   DATE
APPD.   DATE

REV REVISION RECORD
0 NEW RELEASE

DATE NAME
03-21-12 Henry

TITLE 480272M3-C2
(4.3")

DWG. NO.
*120375MA

SHEET 1 OF 1