晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM480272H3TMQW-W0H
APPROVED BY	
DATE	

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2012/2/19	--	New Release 4.3" 480272 LCD + FSA506+i80/16Bit	Kokai

1 Features

4.3 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 4.3” TFT-LCD panel, controller board and backlight unit.

1.1 TFT Panel Feature :

(1) Construction: 4.3” a-Si color TFT-LCD, White LED Backlight and PCB.
(2) Resolution (pixel): 480(R.G.B) X 272
(3) Number of the Colors : 262K colors (R , G , B 6 bit digital each)
(4) LCD type : Transmissive Color TFT LCD (normally White)
(5) Interface: 40 pin pitch 0.5
(6) Power Supply Voltage: 3.3V single power input. Built-in power supply circuit.
(7) Viewing Direction: 6 O’clock (Gray Inversion)

1.2 LCD Controller Feature:

(1) Display RAM size : 640x320x3x6 bits. Ex : 320x240 two frame buffer with 262K colors.
(2) MCU interface : **80-16Bit interface**

2 Physical specifications

Item	Specifications	Unit
Display resolution(dot)	480(R.G.B.) (W) x 272(H)	mm
Active area	95.04 (W) x 53.856 (H)	mm
Screen size	4.3 (Diagonal)	mm
Pixel size	0.198 (W) x 0.198 (H)	um
Color configuration	R.G.B stripe	
Overall dimension	105.5(W) x 67.2(H) x 6.6(D)	mm
Backlight unit	LED	

3. ABSOLUTE MAX. RATINGS

ITEM	SYMBOL	MIN	MAX	UNIT
Operation Temperature	Top	-20	70	℃
Storage Temperature	Tstg	-30	80	℃

4 ELECTRICAL CHARACTERISTICS

4.1 DC Electrical characteristic of the LCD

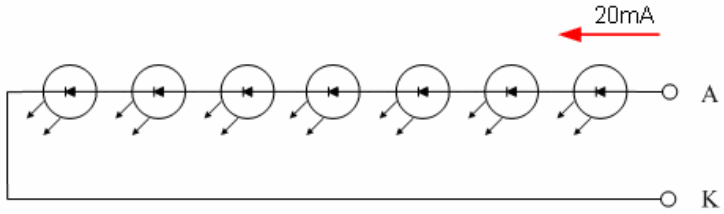
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	5.0	V	
Input Voltage for logic	H Level	V_{IH}	2.0	-	5.5	V	Note 1
	L Level	V_{IL}	VSS	-	0.8	V	
Power Supply current		IDD	-	450	-	mA	Note 2

Note1: With 5V Tolerance Input , /CS, /WR,/RD,RS,DB0~DB17

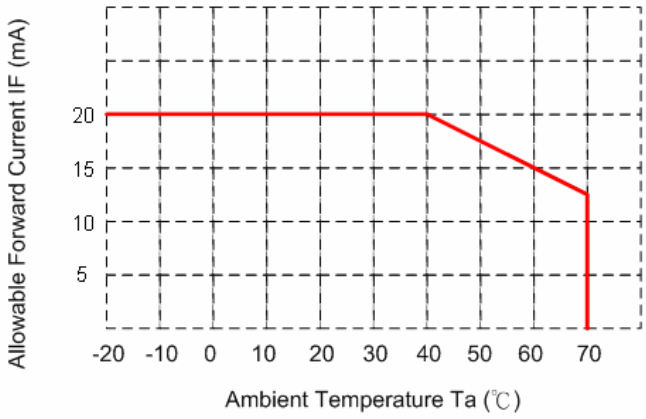
Note2: f =60Hz , Ta=25℃ , Display pattern : All Black ; Including the current for LED driver

4.2 Electrical characteristic of LED Back-light

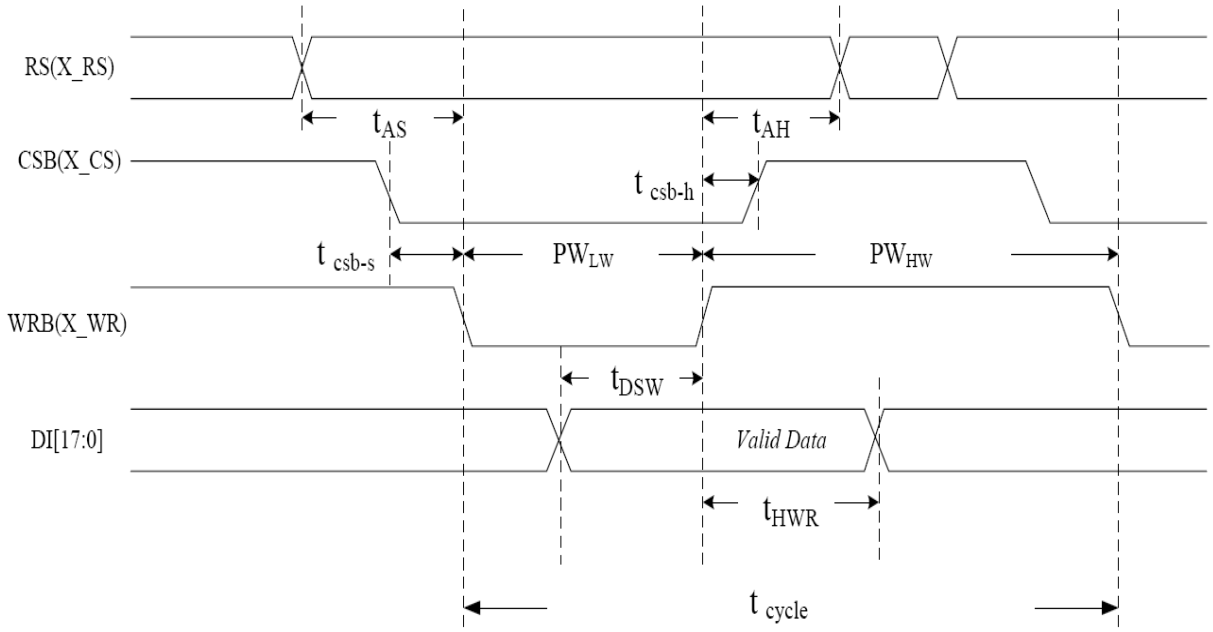
Paramenter	Symbol	Min.	Typ.	Max.	Unit	Condiction
LED voltage	V_{AK}	--	23.1	--	V	I_{LED} =20mA,Ta=25℃
LED forward current	I_{LED}	--	20	--	mA	Ta=25℃
	I_{LED}	--	15	--	mA	Ta=60℃



- The constant current source is needed for white LED back-light driving.
- When LCM is operated over 60℃ ambient temperature, the I_{LED} of the LED back-light should be adjusted to 15 mA.



4.3 AC Timing characteristic of the Graphic TFT LCD controller



Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{cycle}	Enable cycle time	100	200		ns	
PW_{HW}	Enable high-level pulse width	66	70		ns	
PW_{LW}	Enable low-level pulse width	33	130		ns	
t_{AS}	RS setup time	16	25		ns	
t_{AH}	RS hold time	16	45		ns	
t_{DSW}	Write data setup time	50	50		ns	
t_{HWR}	Write data hold time	40	50		ns	
t_{csb-s}	CSB setup time	16	20		ns	
t_{csb-h}	CSB hold time	16	30		ns	

5 OPTICAL SPECIFICATION

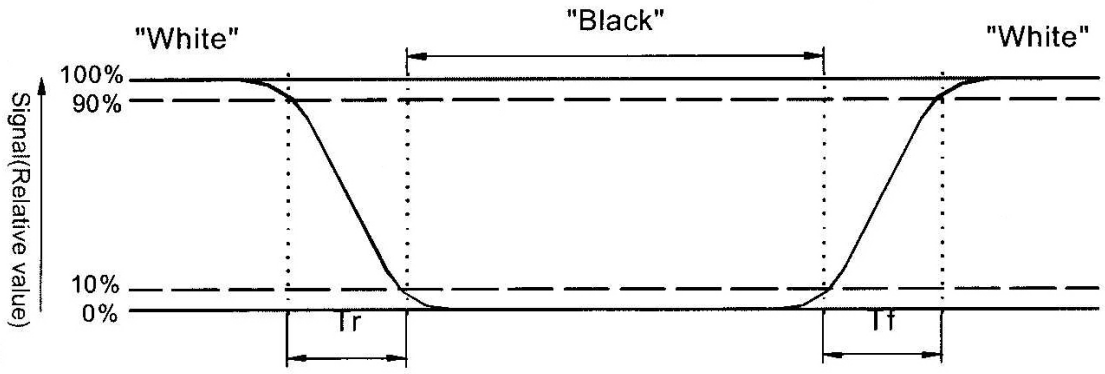
Item		Symbol	Conditon	Min.	Typ.	Max.	Unit	Remark
Response Time	Rise	Tr	Θ=0°	--	15	20	ms	Note 1,2,3
	Fall	Tf		--	35	50		
Contrast ratio		CR	Θ=0°	150	250	--		Note 1,2,4
Viewing Angle	Top		CR≧10	--	55	--	deg.	Note1,2,5
	Bottom			--	35	--		
	Left			--	70	--		
	Right			--	70	--		
Brightness		Y_L	I_{LED}=20mA, 25℃		300	--	cd/m²	Note 6
Red chromaticity		XR	Θ=0°	(0.565)	(0.615)	(0.665)		Note 6
		YR		(0.294)	(0.344)	(0.394)		
Green chromaticity		XG		(0.257)	(0.307)	(0.357)		
		YG		(0.512)	(0.562)	(0.612)		
Blue chromaticity		XB		(0.083)	(0.133)	(0.183)		
		YB		(0.100)	(0.150)	(0.200)		
White chromaticity		XW		(0.259)	(0.309)	(0.359)		
		YW		(0.300)	(0.350)	(0.400)		
Brightness Uniformity			I_{LED}=20mA, 25℃	80	--	--	%	Note 7

Note 1: Ambient temperature=25℃, and LED current I_{LED}=20mA. To be measured in the dark room.

Note 2: To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-7,after 10 minutes operation.

Note 3.Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black“ to “white”(falling time) and from ”white” to “black” (rising time),respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

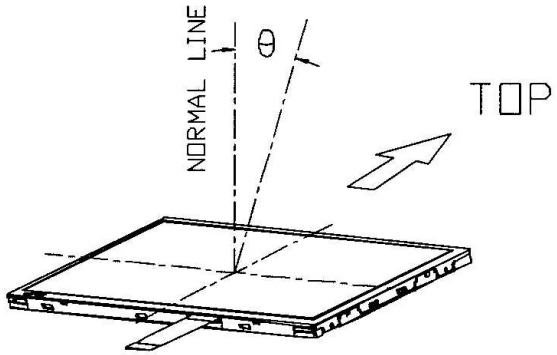


Note 4.Definition of contrast ratio:

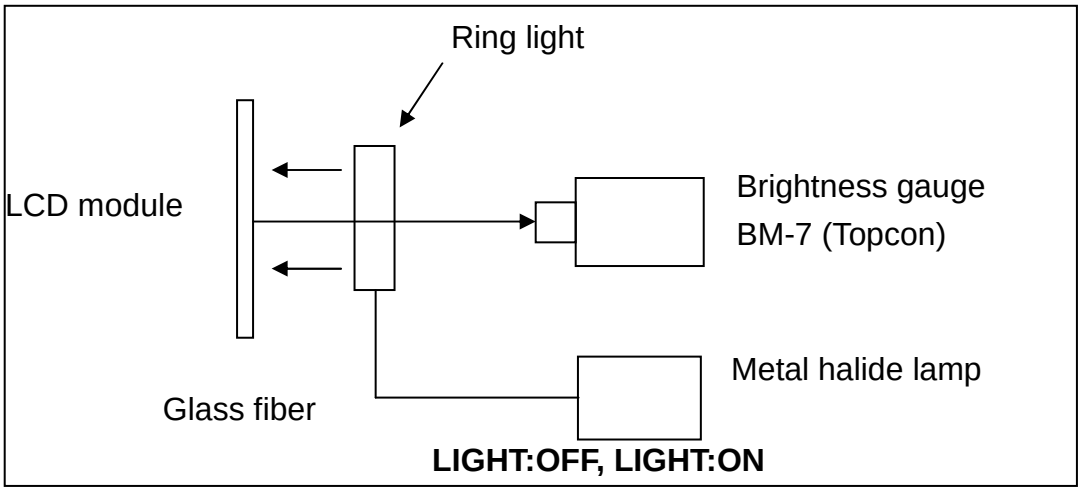
Contrast ratio is calculated with the following formula.

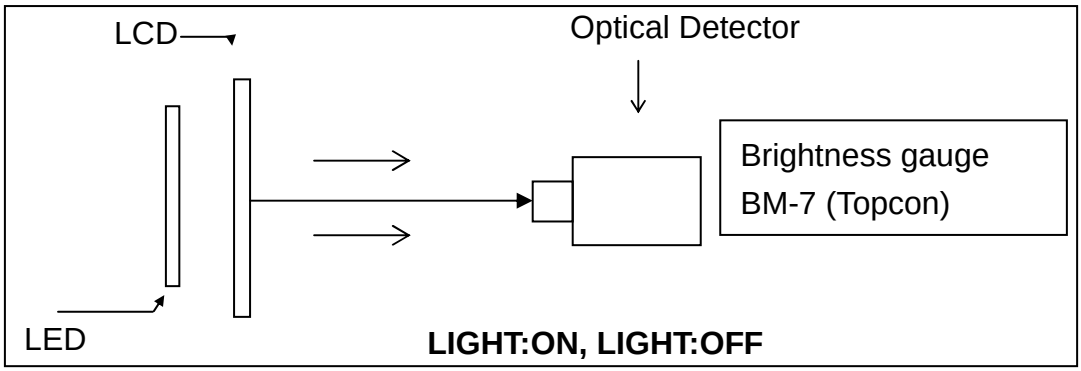
$$\text{Contrast ratio(CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector Output when LCD is at "Black" state}}$$

Note 5.Definition of viewing angle, Refer to figure as below.

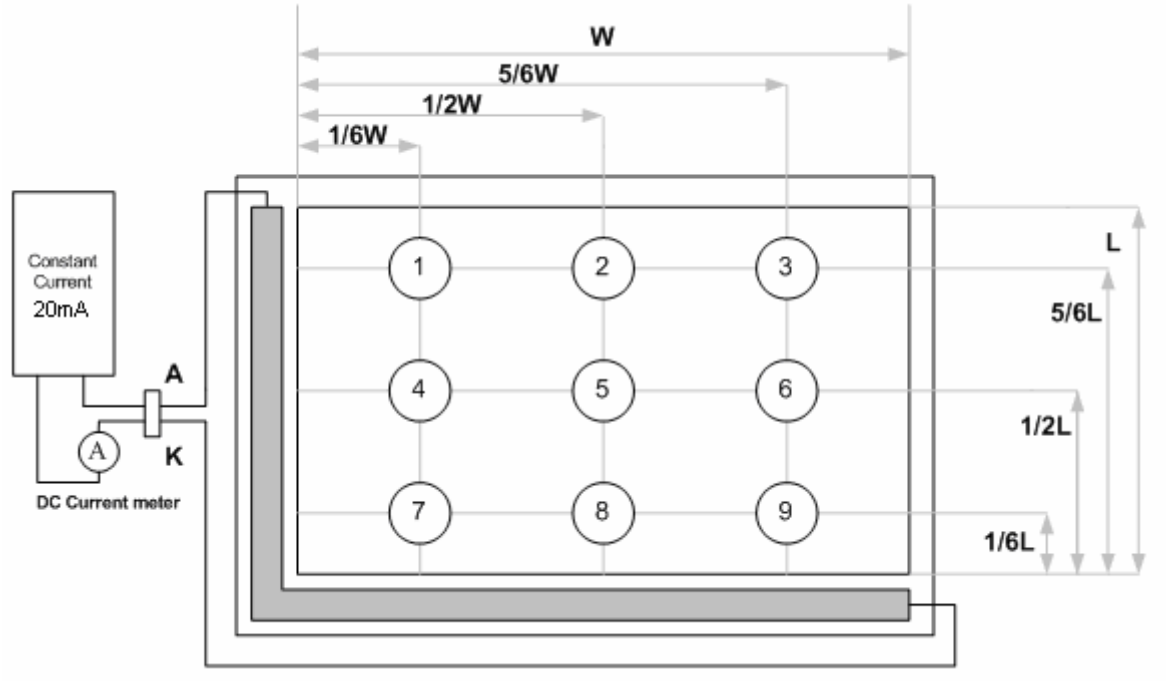


Note 6.Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.





Note 7 : Measurement of the following 9 places on the display.

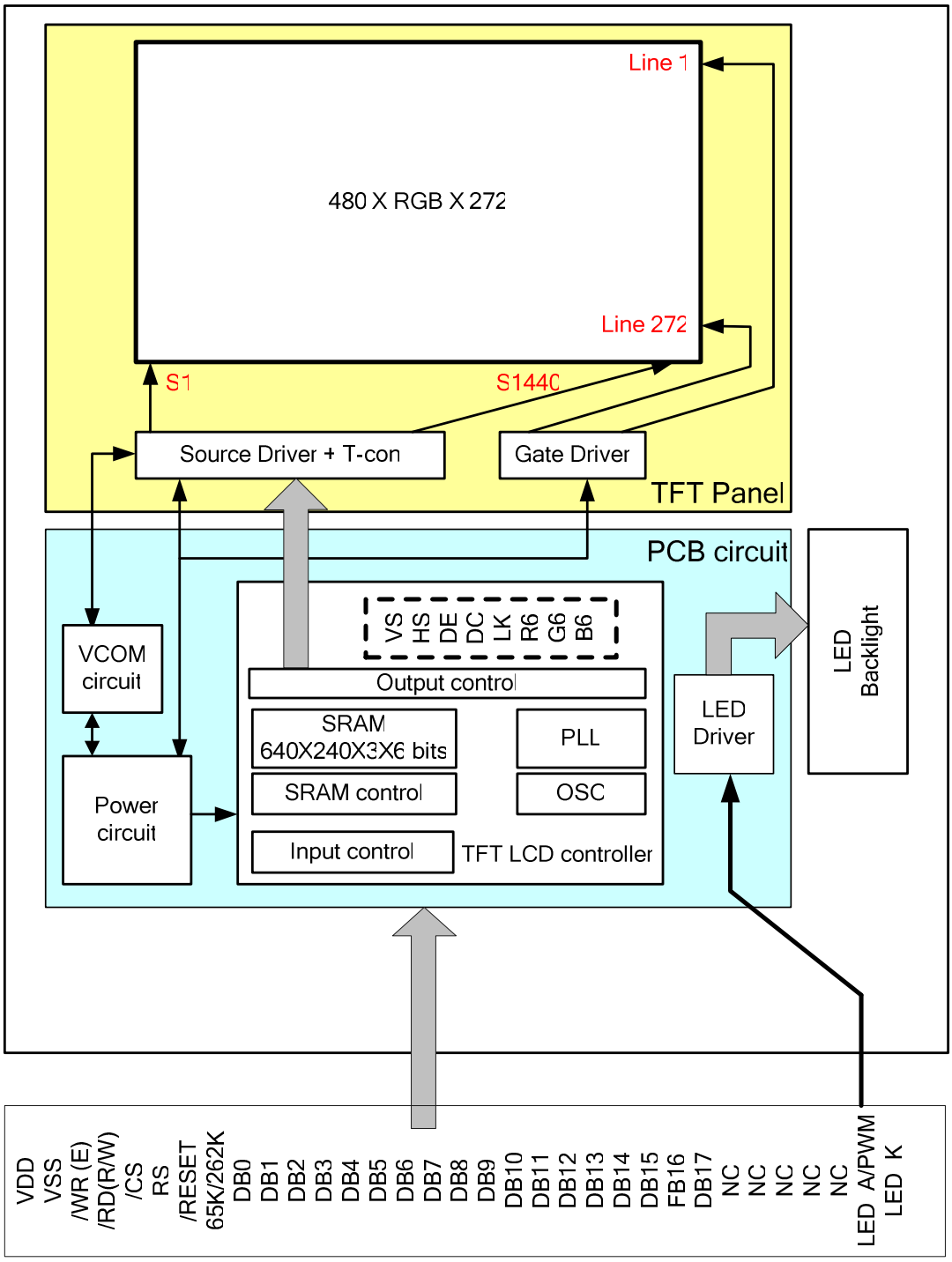


The Uniformity definition : (Min Brightness / Max Brightness) x 100%

6 INTERFACE SPECIFICATIONS

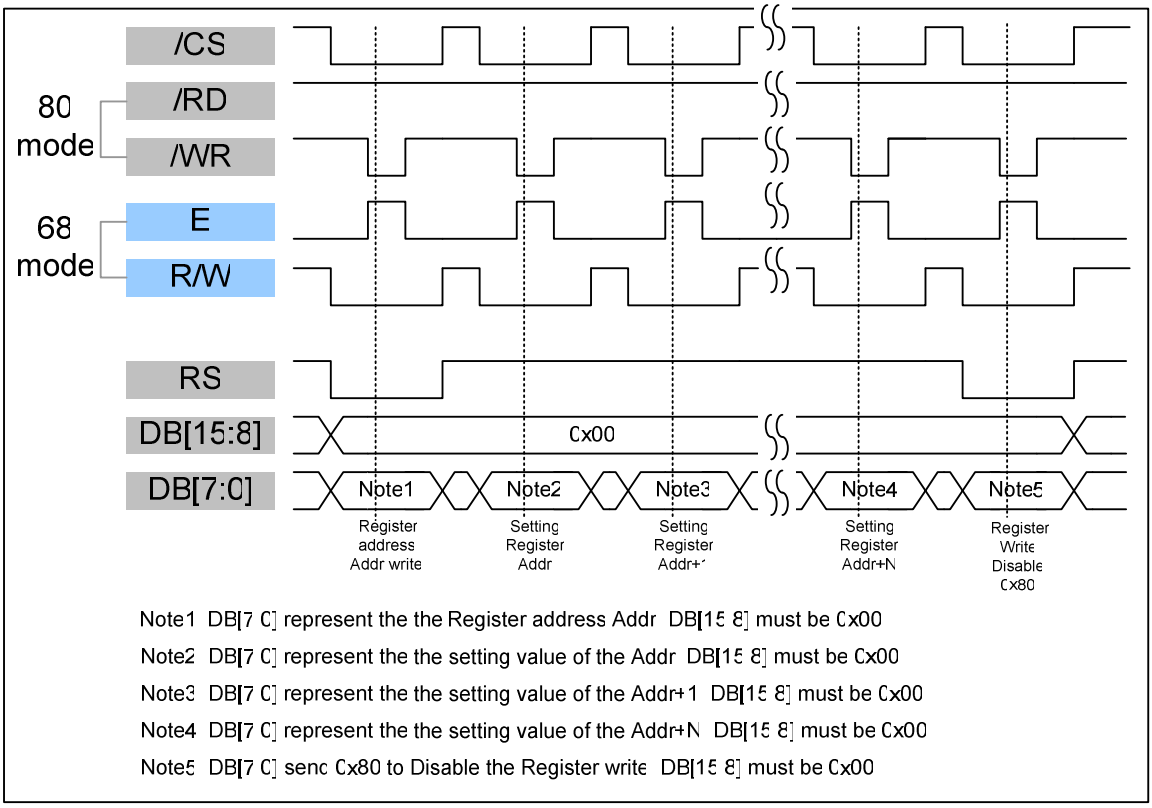
Pin no	Symbol	I/O	Description		Remark
1 ~ 2	VSS		GND		
3	LED_A/PWM		Without LED driver	LED Anode	
			With LED Driver	**PWM**	**Default**
4	LED_K		Without LED driver	LED Cathode	
			With LED Driver	**Must be OPEN**	**Default**
5	/RESET	I	Reset signal for TFT LCD controller		
6	RS	I	Register and Data select for TFT LCD controller		
7	/CS	I	Chip select low active signal for TFT LCD controller		
8	/WR(E)	I	80mode : /WR low active signal for TFT LCD controller 68mode : E signal latch on rising edge		
9	/RD(R/W)	I	80mode : /RD low active signal for TFT LCD controller 68mode : R/W signal Hi: read Lo:Write		
10 ~ 27	DB0 ~ DB17	I/O	Data Bus		
28	65K/262K	I	Select colors data format H : 262K L : 65K		
29	VSS		GND		
30	XR		No connection		
31	XL		No connection		
32	YD		No connection		
33	YU		No connection		
34	NC		No connection		
35 ~ 37	VDD		Power supply for the logic (3.3V)		
38 ~ 40	VSS		GND		

7 BLOCK DIAGRAM



8 INTERFACE PROTOCOL

8-1 16Bit-80/68- Write to Command Register



Note1 DB[7:0] represent the the Register address Addr DB[15:8] must be Cx00

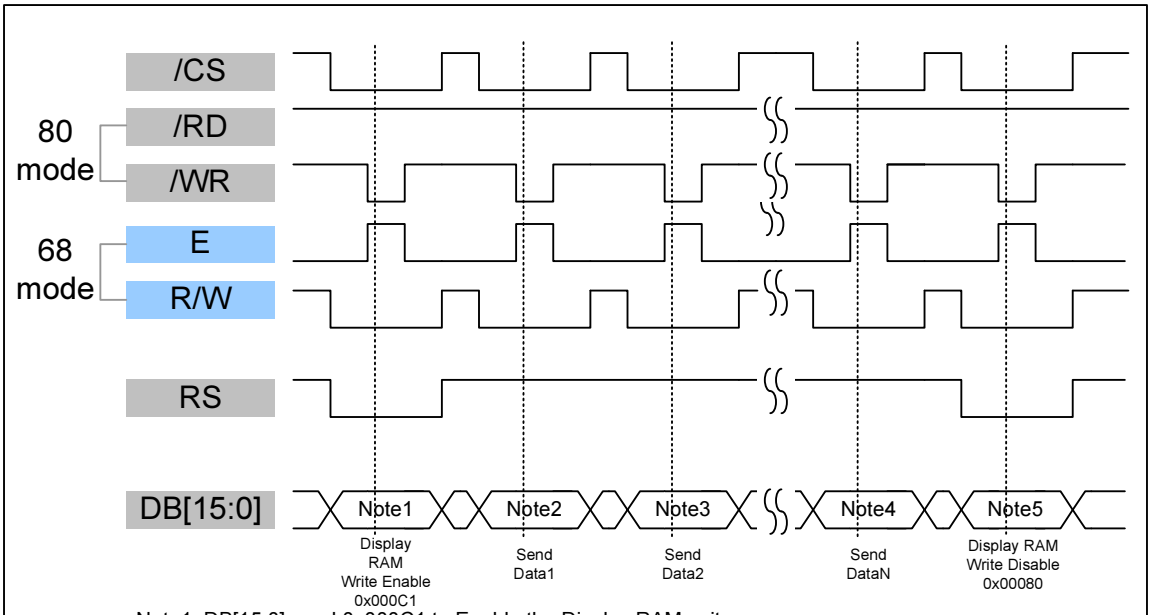
Note2 DB[7:0] represent the the setting value of the Addr DB[15:8] must be Cx00

Note3 DB[7:0] represent the the setting value of the Addr+1 DB[15:8] must be Cx00

Note4 DB[7:0] represent the the setting value of the Addr+N DB[15:8] must be Cx00

Note5 DB[7:0] senc Cx80 to Disable the Register write DB[15:8] must be Cx00

8-2 16Bit-80/68-Write to Display RAM



Note1: DB[15:0] send 0x000C1 to Enable the Display RAM write.

Note2: DB[15:0] represent the writing Data1 to Display RAM

Note3: DB[15:0] represent the writing Data2 to Display RAM

Note4: DB[15:0] represent the writing DataN to Display RAM

Note5: DB[15:0] send 0x00080 to Disable the Display RAM write.

8-3Data transfer order Setting

8-3.1 16 bit interface 65K color (Pin28 65K/262K =Low)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

8-3.2 16 bit interface 262K color (Pin28 65K/262K =High)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	X	X	X	X	X	X	X	R5	R4
2nd data	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

9 REGISTER DESCRIPTION

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
00	00	MSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
01	00	LSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
02	01	MSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
03	3F	LSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
04	00	MSB of Y-axis start position								
Description	set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
05	00	LSB of Y-axis start position								
Description	Set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
06	00	MSB of Y-axis end position								
Description	set the vertical end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
07	EF	LSB of Y-axis end position								
Description	Set the vertical end position of display active region									

To simplify the address control of display RAM access, the window area address function allows for writing data only within a window area of display RAM specified by registers REG[00]~REG[07] .

After writing data to the display RAM, the Address counter will be increased within setting window address-range which is specified by

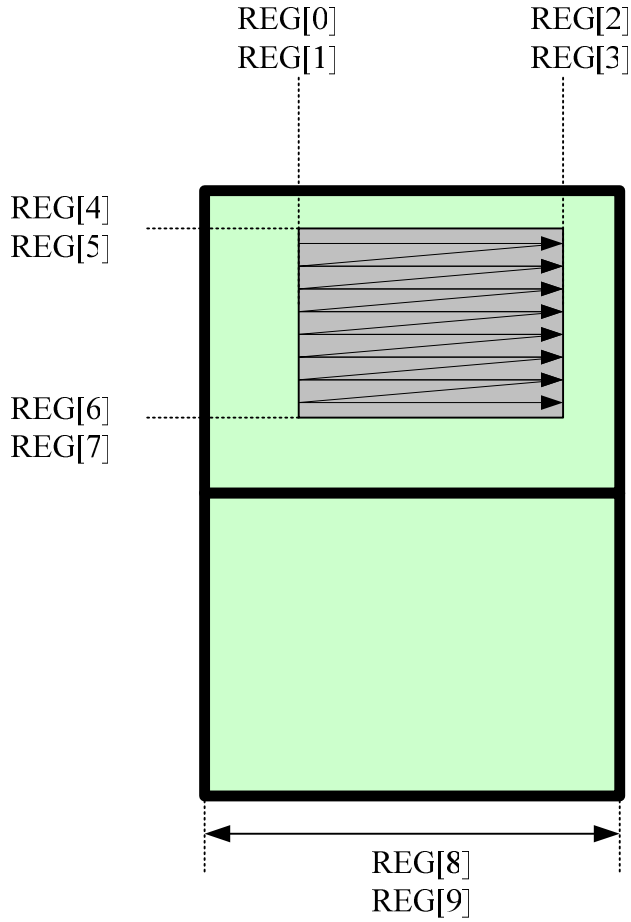
MIN X address (REG[0] & REG[1])

MAX X address (REG[2] & REG[3])

MIN Y address (REG[4] & REG[5])

MAX Y address (REG[6] & REG[7])

Therefore, data can be written consecutively without thinking the data address.



Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
08	01	X	X	X	X	X	X	_PanelXSize H_Byte[1:0]		
Description	Set the panel X size									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
09	40	_PanelXSize L_Byte[7:0]								
Description	Set the panel X size									

The register REG[08] and REG[09] is use to calculate the RAM address. If you want to use the TFT as Landscape mode (320x240), the REG[08] & RGE[09 must set to 320. If you want to use the TFT as Portrait mode (240x320), the REG[08] & RGE[09] must set to 240.

Register Address	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark

(Hex)										
0A	00	X	X	X	X	X	[17:16] bits of memory write start address			
Description	Memory write start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0B	00	[15:8] bits of memory write start address								
Description	Memory write start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0C	00	[7:0] bits of memory write start address								
Description	Memory write start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x10	0x0D	Bit_SWAP	OUT_TEST	BUS_SEL		Blanking	P/S_SEL	CLK_SEL		
Description	"0x10_Clk_sel[1:0]" : The TFT controller built-in 40Mhz PLL clock. These bits are for select the TFT panel dot clock frequency. 00 : 20Mhz 01: 10Mhz 02: 5 Mhz									
	"0x10_ps_sel[2]" : The TFT controller support parallel and serial RGB interface. These bits are for select the output timing. 0 : serial Panel 1: Parallel panel									
	"0x10_blanking_tmp[3]" 0 : OFF (blanking) 1: ON (normal operation)									
	"0x10_bus_sel[5:4]" : It only for serial Panel 00=R , 01=G , 10=B									
	"0x10_out_test[6]" : Self test 0 : normal operation 1: for test (don't use for normal operation) When set the bit to "1" , the Rout=(Reg 2a[6:0]) Gout=(Reg 2b[6:0]) Bout=(Reg 2c[6:0])									
	"0x10_bit_swap[7]" : 0-normal									
	The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x11	00	X	X	EVEN			_ODD			
Description	" Even line of serial panel data out sequence or data bus order of parallel panel 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved									

	Odd line of serial panel data out sequence 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG **101: BGR** Others: reserved **Must Set to 0x05 for AM320240N1**

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x12	00					Hsync_stH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x13	00	Hsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x14	00					Hsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x15	10	Hsync_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x16	00					Hact_stH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x17	38	Hact_stL_Byte[7:0]								

Description	For TFT output timing adjust: DE pulse start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x18	01					Hact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x19	40	Hact_pwL_Byte[7:0]								
Description	For TFT output timing adjust: DE pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1A	01					HtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync total clocks H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1B	B8	HtotalL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync total clocks H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1C	00					Vsync_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1D	00	Vsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark

(Hex)										
0x1E	00					Vsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1F	08	Vsync_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x20	00					Vact_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical DE pulse start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x21	12	Vact_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical DE pulse start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x22	00					Vact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical Active width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x23	F0	Vact_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical Active width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x24	01					VtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical total width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x25	09	VtotalL_Byte[7:0]								

Description	For TFT output timing adjust: Vertical total width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.

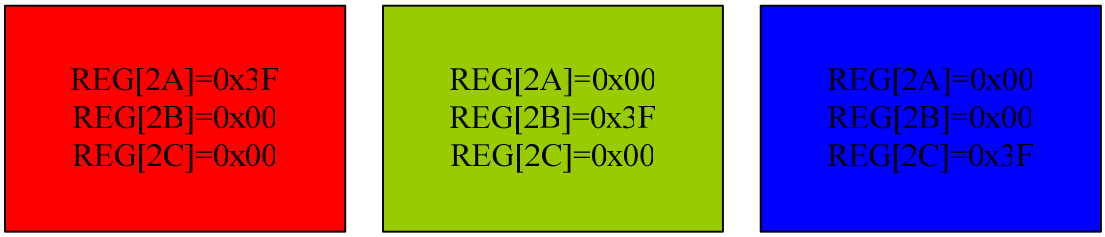
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
26	00	X	X	X	X	X	[17:16] bits of memory read start address			
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
27	00	[15:8] bits of memory write start address								
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
28	00	[7:0] bits of memory write start address								
Description	Memory read start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
29	00	[7:1] Reversed								
Description	[0] Load output timing related setting (H sync., V sync. and DE) to take effect									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2A	00	X	TestPatternRout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Rout data equal to TestPatternRout[6:0]									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2B	00	X	TestPatternGout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Gout data equal to TestPatternGout[6:0]									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2C	00	X	TestPatternBout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Bout data equal to TestPatternBout[6:0]									

If you set the " REG[0x10]_out_test[6]" : Self test =1 , the TFT controller will skip the

connect of the display RAM. The Output port will send the REG[2A] ,REG[2B],REG[2C] data.



Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2D	00	X	X	X	X	[3]	Rising/falling edge[2]	_rotate [1:0]		
Description	[3] Output pin X_DCON level control ; TFT Power ON/OFF control 0: TFT POWER circuit OFF 1: TFT POWER circuit ON									
	Rising/falling edge[2] : 0: The RGB out put data are on the Rising edge of the DCLK. 1: The RGB out put data are on the Falling edge of the DCLK.									
	_rotate [1:0]: 00 : rotate 0 degree 01 : rotate90 degree 10 : rotate 270 degree 11 : rotate 180 degree									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
30	00	X	X	X	X	X	_H byte H-Offset[3:0]			
Description	Set the Horizontal offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
31	00	_L byte H-Offset[7:0]								
Description	Set the Horizontal offset									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
32	00	X	X	X	X	X	_H byte V-Offset[3:0]			
Description	Set the Vertical offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark

33	00	_L byte V-Offset[7:0]	
Description	Set the Vertical offset		

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
34	00	[7:4] Reserved					_H byte H-def[3:0]			
Description	[3:0] MSB of image horizontal physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
35	40	_L byte H-def[7:0]								
Description	[7:0] LSB of image horizontal physical resolution in memory									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
36	01	[7:4] Reserved					_H byte V-def[3:0]			
Description	[3:0] MSB of image vertical physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
37	E0	_L byte V-def[7:0]								
Description	[7:0] LSB of image vertical physical resolution in memory									

The total RAM size is 640x240x18bit. The user can arrange the Horizontal ram size by REG[34],REG[35] and the Vertical ram size by REG[36],REG[37].

EX: 320x480x18bit REG[34]=0x01 , REG[35]=0x40 , REG[36]=0x01 , REG[37]=0xE0

EX: 640x240x18bit. REG[34]=0x02 , REG[35]=0x80 , REG[36]=0x00 , REG[37]=0xF0

DISPLAYED COLOR AND INPUT DATA

	Color & Gray Scale	DATA SIGNAL																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(31)	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(61)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(31)	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(1)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(31)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

10 QUALITY AND RELIABILITY

1. Scope

Specifications contain

1.1 Display Quality Evaluation

1.2 Mechanics Specification

2. Sampling Plan

Unless there is other agreement, the sampling plan for incoming inspection shall follow MIL-STD-105E LEVEL II.

2.1 Lot size: Quantity per shipment as one lot (different model as different lot).

2.2 Sampling type: Normal inspection, single sampling.

2.3 Sampling level: Level II.

2.4 AQL: Acceptable Quality Level

Major defect: AQL=0.65

Minor defect: AQL=1.0

3. Panel Inspection Condition

3.1 Environment:

Room Temperature: 25±5°C.

Humidity: 65±5% RH.

Illumination: 300 ~ 700 Lux.

3.2 Inspection Distance:

35-40 cm

3.3 Inspection Angle:

The vision of inspector should be perpendicular to the surface of the Module.

3.4 Inspection time：

Perceptibility Test Time: 20 seconds max.

4. Display Quality

4.1 Function Related:

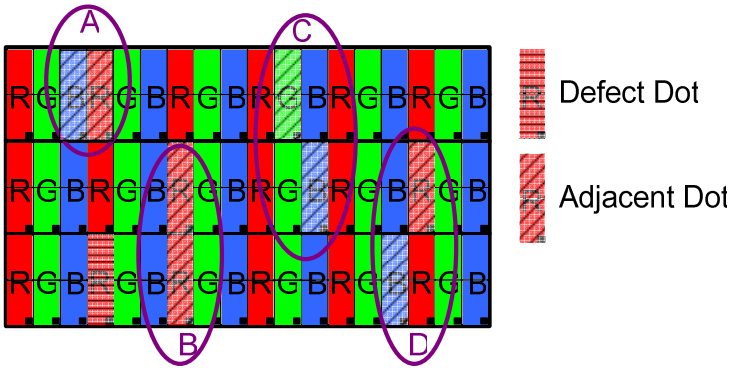
The function defects of line defect, abnormal display, and no display are considered Major defects.

4.2 Bright/Dark Dots:

Defect Type / Specification	G0 Grade	A Grade
Bright Dots	0	N≤ 1
Dark Dots	0	N≤ 3
Total Bright and Dark Dots	0	N≤ 3

[Note 1]

Judge defect dot and adjacent dot as following.



(1) One pixel consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot)

(2) The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.

(3) Allow above (as A, B, C and D status) adjacent defect dots, including bright and dart adjacent dot. And they will be counted 2 defect dots in total quantity.

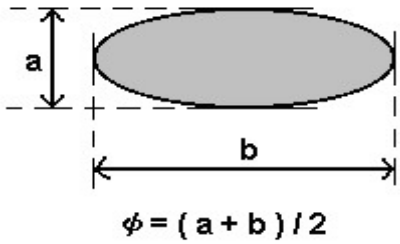
(4) Defects on the Black Matrix, out of Display area, are not considered as a defect or counted.

(5) There should be no distinct non-uniformity visible through 6% ND Filter within 2 sec inspection times.

4.3 Visual Inspection specifications:

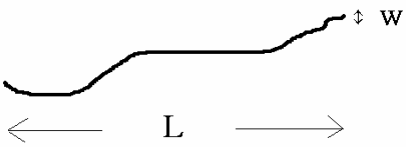
Defect Type	Specification	Count(N)
Dot Shape (Particle、Scratch and Bubbles in display area)	D≤0.15mm	Ignored
	0.15mm < D≤ 0.3mm	N≤ 3
	D > 0.3mm	N=0
Line Shape (Particles、Scratch、Lint and Bubbles in display area)	W≤ 0.05mm	Ignored
	0.05mm<W≤ 0.1mm ， L≤ 3mm	N≤ 3
	W > 0.1mm ， L > 3mm	N=0

[Note 2] W : Width[mm], L : Length[mm], N : Number, φ : Average Diameter



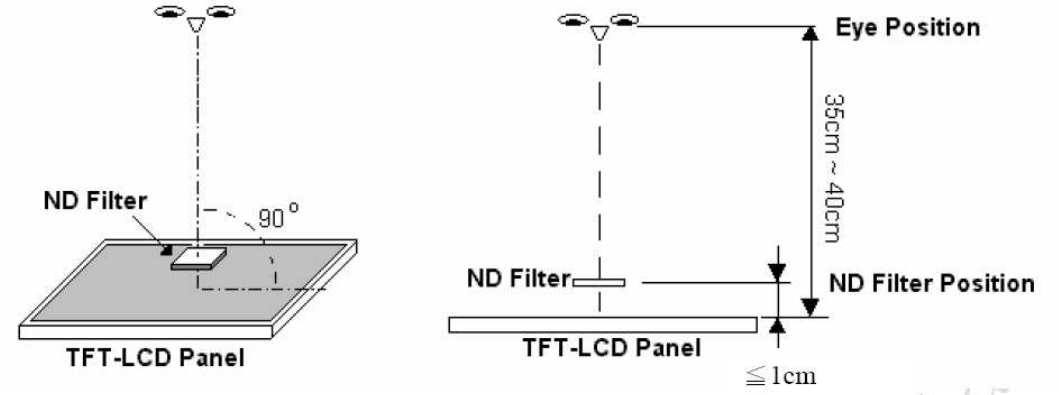
$\phi = (a + b) / 2$

1. (White, black) Spot
2. Polarizer Bubble



1. fiber

[Note 3] Bright dot is defined through 6% transmission ND Filter as following.



11 RELIABILITY TEST CONDITIONS

ITEM	CONDITIONS	NOTE
HIGH TEMPERATURE OPERATION	70℃ , 240Hrs	
HIGH TEMPERATURE AND HIGH HUMIDITY OPERATION	60℃ , 90%RH , 240Hrs	
HIGH TEMPERATURE STORAGE	80℃ , 240Hrs	
LOW TEMPERATURE OPERATION	-20℃ , 240Hrs	
LOW TEMPERATURE STORAGE	-30℃ , 240Hrs	
THERMAL SHOCK	-30℃(1Hr) ~80℃(1Hr) 200Cycle	

12 USE PRECAUTIONS

12-1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

12-2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

12-3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0℃ and 35℃ and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

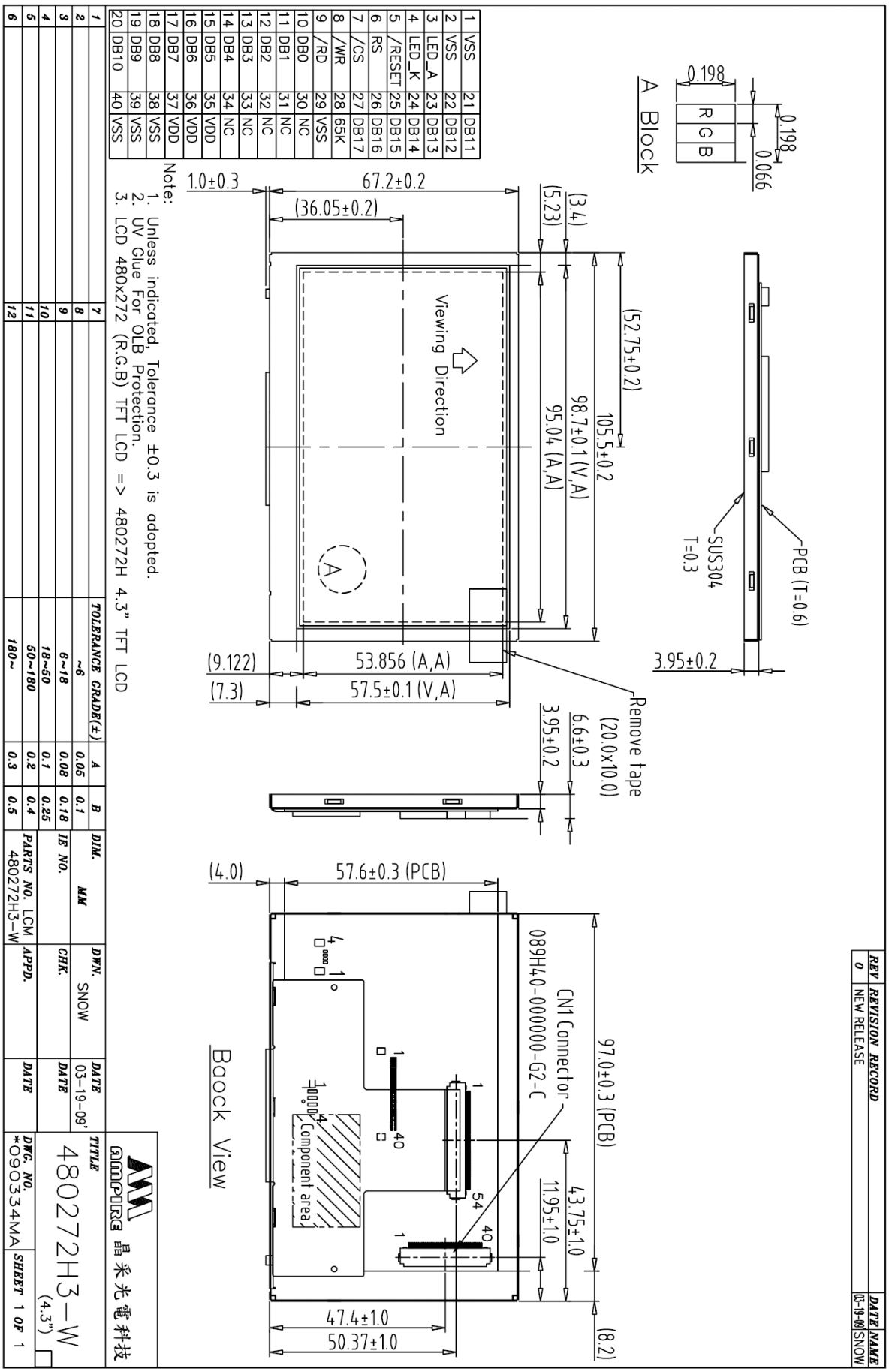
12-4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

12-5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

13 OUTLINE DIMENSION



1	VSS	21	DB11																		
2	VSS	22	DB12																		
3	LED_A	23	DB13																		
4	LED_K	24	DB14																		
5	/RESET	25	DB15																		
6	RS	26	DB16																		
7	/CS	27	DB17																		
8	/WR	28	65K																		
9	/RD	29	VSS																		
10	DB0	30	NC																		
11	DB1	31	NC																		
12	DB2	32	NC																		
13	DB3	33	NC																		
14	DB4	34	NC																		
15	DB5	35	VDD																		
16	DB6	36	VDD																		
17	DB7	37	VDD																		
18	DB8	38	VSS																		
19	DB9	39	VSS																		
20	DB10	40	VSS																		

Note:
1. Unless indicated, Tolerance ±0.3 is adopted.
2. UV Glue For OLB Protection.
3. LCD 480x272 (R.G.B) TFT LCD => 480272H 4.3" TFT LCD

REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	03-19-09	SNOW

TOLERANCE	GRADE(±)	A	B
~6		0.05	0.1
6~18		0.08	0.18
18~50		0.1	0.25
50~180		0.2	0.4
180~		0.3	0.5

DIM. MM
IE NO.
PARTS NO. LCM 480272H3-W

DWN. SNOW DATE 03-19-09'
CHK. DATE
APPD. DATE

AMPIRE 晶采光電科技

TITLE 480272H3-W (4.3")

DWG. NO. *09033-4MA

SHEET 1 OF 1