晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM-320240L8TNQW-C0H
APPROVED BY	
DATE	

☐ Approved For Specifications
☐ Approved For Specifications & Sample

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2008/10/28	-	New Release	Edward
2011/3/29	8	Viewing angle update	Patrick

1 Features

3.5 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 3.5" TFT-LCD panel, LCD controller and power driver circuit, LED driver circuit and backlight unit.

1.1 TFT Panel Feature :

(1) Construction: 3.5" a-Si color TFT-LCD, White LED Backlight and PCB.
(2) Resolution (pixel): 320(R.G.B) X240
(3) Number of the Colors : 262K colors (R , G , B 6 bit digital each)
(4) LCD type : Transmissive Color TFT LCD (normally White)
(5) Interface: 40 pin pitch 0.5 FFC
(6) Power Supply Voltage: 3.3V single power input. Built-in power supply circuit.

1.2 LCD Controller Feature:

(1) MCU interface: 16 bit 80 series MCU interface.
(2) Display RAM size: 640x240x3x6 bits. Ex: 320x240 two frame buffer with 262K colors.
(3) Arbitrary display memory starts position selection.
(4) 16 bit interface support 65K (R5 G6 B5) Color.

2 Physical specifications

Item	Specifications	Unit
Display resolution(dot)	960 (W) x 240(H)	dot
Active area	70.08(W) x 52.56(H)	mm
Screen size	3.5(Diagonal)	mm
Pixel size	73 (W) x 219 (H)	um
Color configuration	R.G.B stripe	
Overall dimension	77.8(W)x64.5(H) x5.85(D)	mm
Viewing Direction	6 o'clock (Gray Inversion)	
Backlight unit	LED	

3 Electrical specification

3.1 Absolute max. ratings

3.1.1 Electrical Absolute max. ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDD	VSS=0	-0.3	5.5	V	
Input voltege	V_{in}		-0.3	VDD+0.3	V	Note 1

Note1: /CS,/WR,/RD,RS,DB0~DN17

3.1.2 Environmental Absolute max. ratings

Item	OPERATING		STORAGE		Remark
	MIN	MAX	MIN	MAX	
Temperature	-20	70	-30	80	Note2,3,4,5,6,7
Humidity	Note1		Note1		
Corrosive Gas	Not Acceptable		Not Acceptable		

Note1 : Ta <= 40℃ : 85% RH max

Ta > 40℃ : Absolute humidity must be lower than the humidity of 85%RH at 40℃

Note2 : For storage condition Ta at -30℃ < 48h , at 80℃ < 100h

For operating condition Ta at -20℃ < 100h

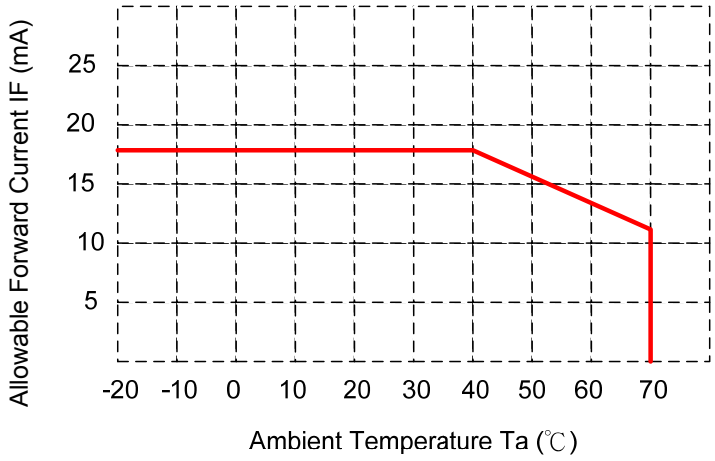
Note3 : Background color changes slightly depending on ambient temperature. This phenomenon is reversible.

Note4 : The response time will be slower at low temperature.

Note5 : Only operation is guarantied at operating temperature. Contrast , response time, another display quality are evaluated at +25℃

Note6 :

- LED BL : When LCM is operated over 40℃ ambient temperature, the I_{LED} of the LED back-light should be follow :



Note7 : This is panel surface temperature, not ambient temperature.
Note8 :

- LED BL: When LCM is operated over than 40℃, the life time of the LED back-light will be reduced.

3.1.3 LED back-light Unit Absolute max. ratings

Item	Symbol	Ratings	Unit	Remark
Peak forward Current	IF	60	mA	
Reverse Voltage	VR	15	V	
Power Dissipation	Po	0.9	W	

3.2 Electrical characteristics

3.2.1 DC Electrical characteristic of the LCD

Typical operting conditions (VSS=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	5.0	V	
Input Voltage for logic	H Level	V_{IH}	2.0	-	5.5	V	Note 1
	L Level	V_{IL}	VSS	-	0.8	V	
Output Voltage for Logic	H Level	V_{OH}	2.4	-	VDD	V	Note 2
	L Level	V_{OL}	VSS		0.4	V	
Power Supply current		IDD	-	320	-	mA	Note 3

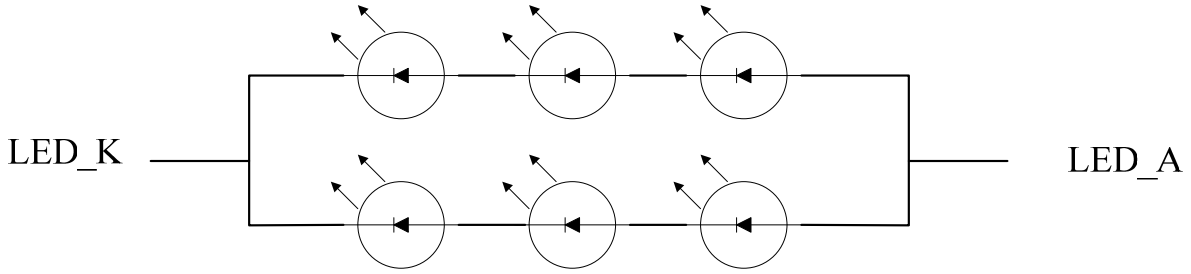
Note1: With 5V Tolerance Input, /CS, /WR,/RD,RS,DB0~DB17

Note2: DB0~DB17

Note3: fV =60Hz, Ta=25℃, Display pattern: All Black

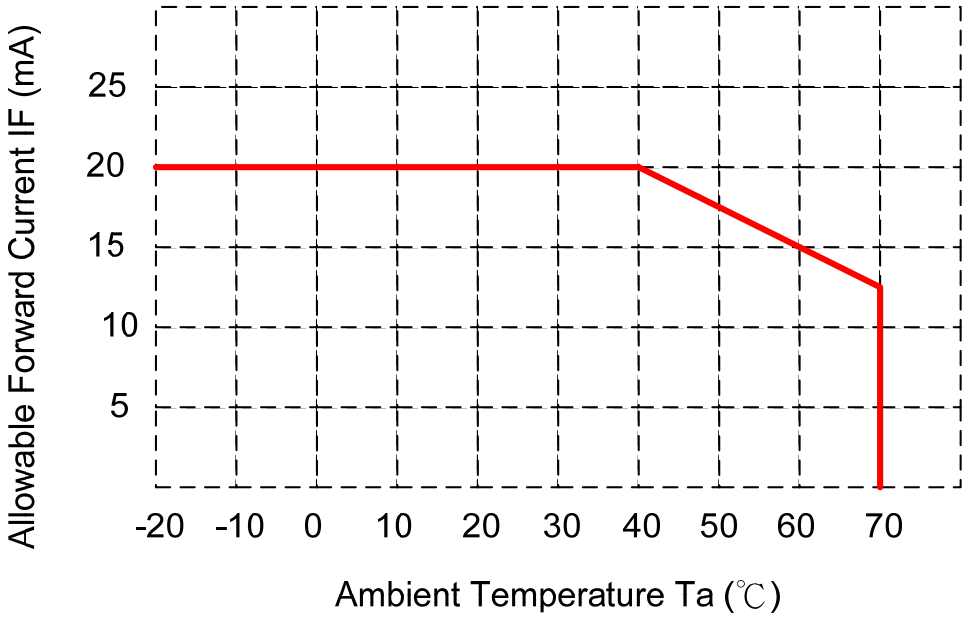
3.2.2 Electrical characteristic of LED Back-light

Paramenter	Symbol	Min.	Typ.	Max.	Unit	Condiction
LED voltage	V_{AK}	--	9.6	--	V	I_{LED} =40mA
LED forward current	I_{LED}	--	40	--	mA	Ta=25℃
	I_{LED}	--	30	--	mA	Ta=60℃

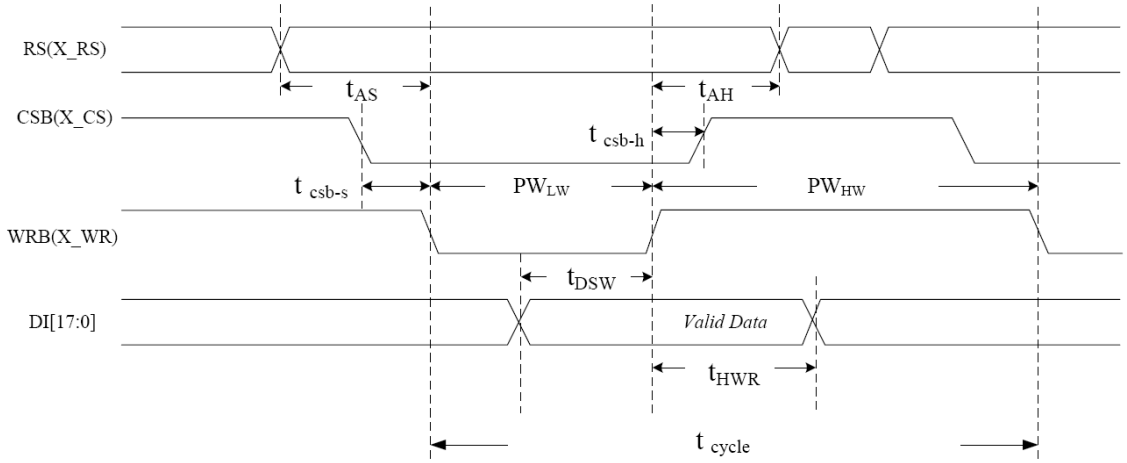


■ The constant current source is needed for white LED back-light driving.

When LCM is operated over 60℃ ambient temperature, the I_{LED} of the LED back-light should be adjusted to 15mA max(For one dice LED).



3.3 AC Timing characteristic of the Graphic TFT LCD controller



Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{cycle}	Enable cycle time	100	200		ns	
PW_{HW}	Enable high-level pulse width	66	70		ns	
PW_{LW}	Enable low-level pulse width	33	130		ns	
t_{AS}	RS setup time	16	25		ns	
t_{AH}	RS hold time	16	45		ns	
t_{DSW}	Write data setup time	50	50		ns	
t_{HWR}	Write data hold time	50	40		ns	
t_{csb-s}	CSB setup time	16	20		ns	
t_{csb-h}	CSB hold time	16	30		ns	

4 Optical specification

4.1 Optical characteristic:

Item		Symbol	Conditon	Min.	Typ.	Max.	Unit	Remark
Response Time	Rise + Fall	T_r+T_f	Θ=0°		25	40	ms	Note 1,2,3,5
Contrast ratio		CR	At optimized viewing angle	200	300	-		Note 1,2,4,5
Viewing Angle	Top Bottom Left Right		CR≧10	- - - -	50 70 70 70	- - - -	deg.	Note1,2, 5,6
Brightness LED BL Without TP		Y_L	I_{LED}=40mA ,25℃	--	500	-	cd/ m^2	Note 7
Red chromaticity		XR		0.57	0.61	0.65		Note 7
		YR		0.32	0.36	0.40		
Green chromaticity		XG		0.31	0.35	0.39		
		YG		0.54	0.58	0.62		
Blue chromaticity		XB		0.10	0.14	0.20		
		YB		0.03	0.07	0.11		
White chromaticity		XW		0.25	-	0.35		
		YW		0.26	-	0.36		

Note 1:

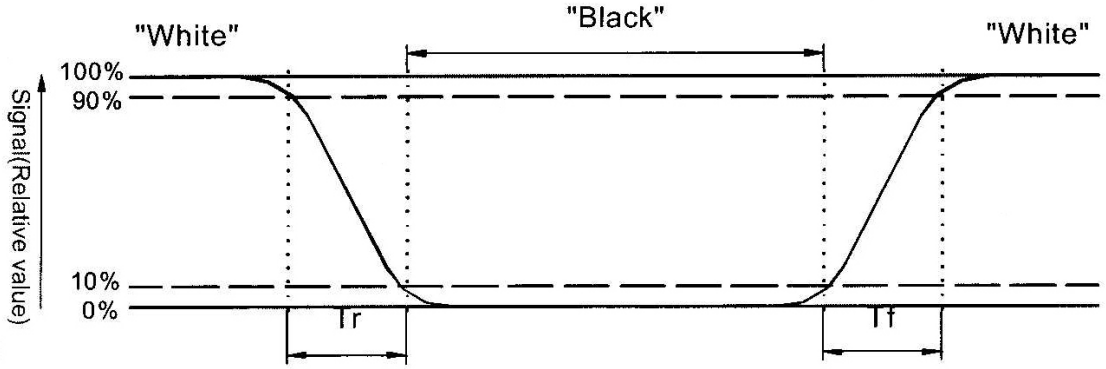
- LED BL :Ambient temperature=25℃,and lamp current I_{LED}=40mA.To be measured in the dark room.

Note 2:To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-7,after 10 minutes operation.

Note 3.Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black“ to “white”(falling time) and from “white” to “black”

(rising time),respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio(CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector Output when LCD is at "Black" state}}$$

Note 5:White $V_i = V_{i50} + 1.5V$

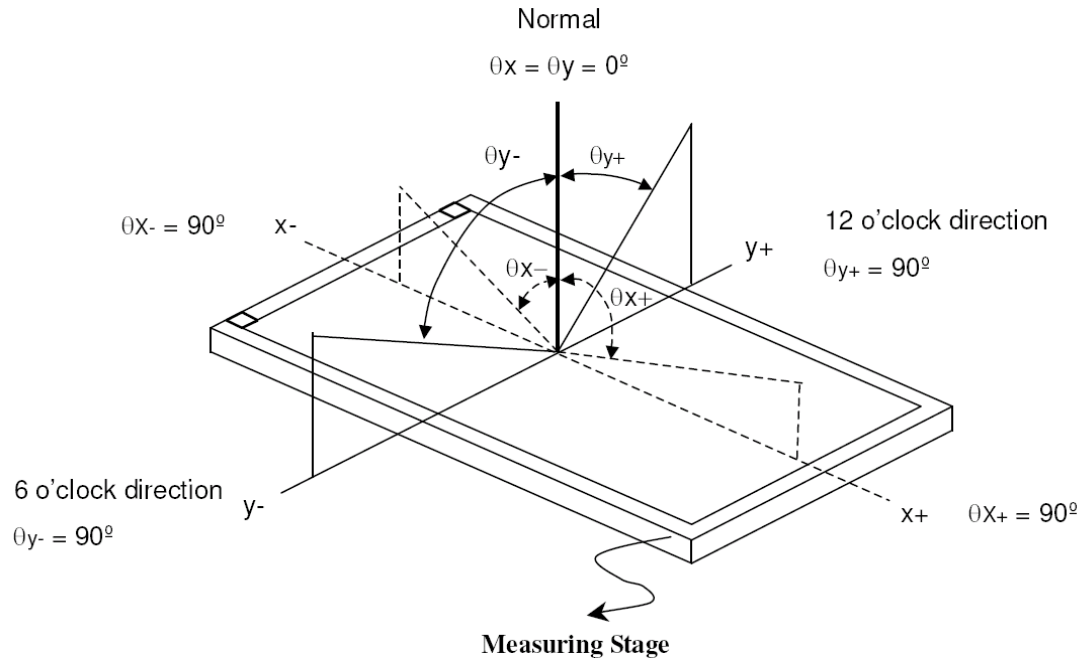
Black $V_i = V_{i50} + 2.0V$

"±"means that the analog input signal swings in phase with V_{COM} signal.

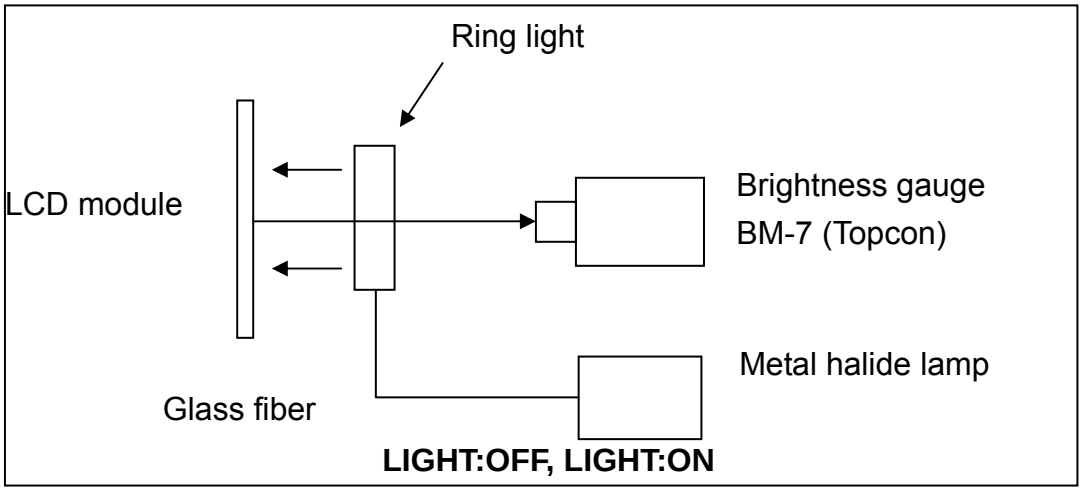
"$\frac{-}{+}$" means that the analog input signal swings out of phase with V_{COM} signal.

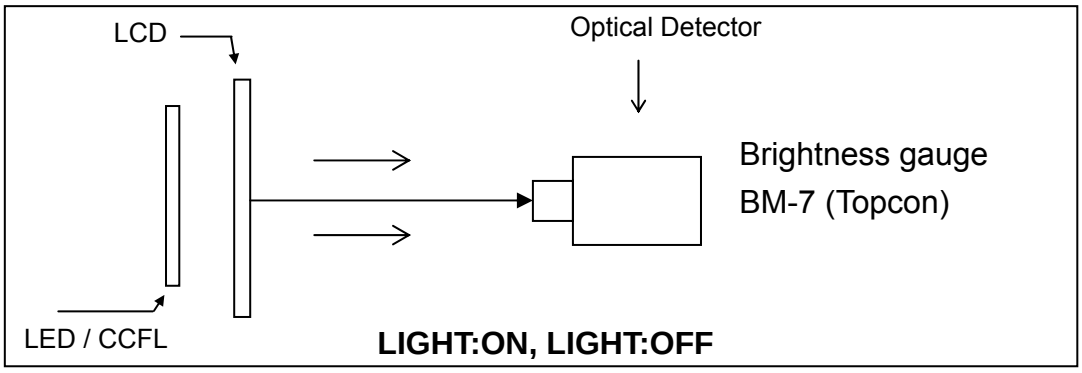
V_{i50} : The analog input voltage when transmission is 50%.The 100% Transmission is defined as the transmission of LCD panel when all the Input terminals of module are electrically opened.

Note 6.Definition of viewing angle, Refer to figure as below.



Note 7.Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.





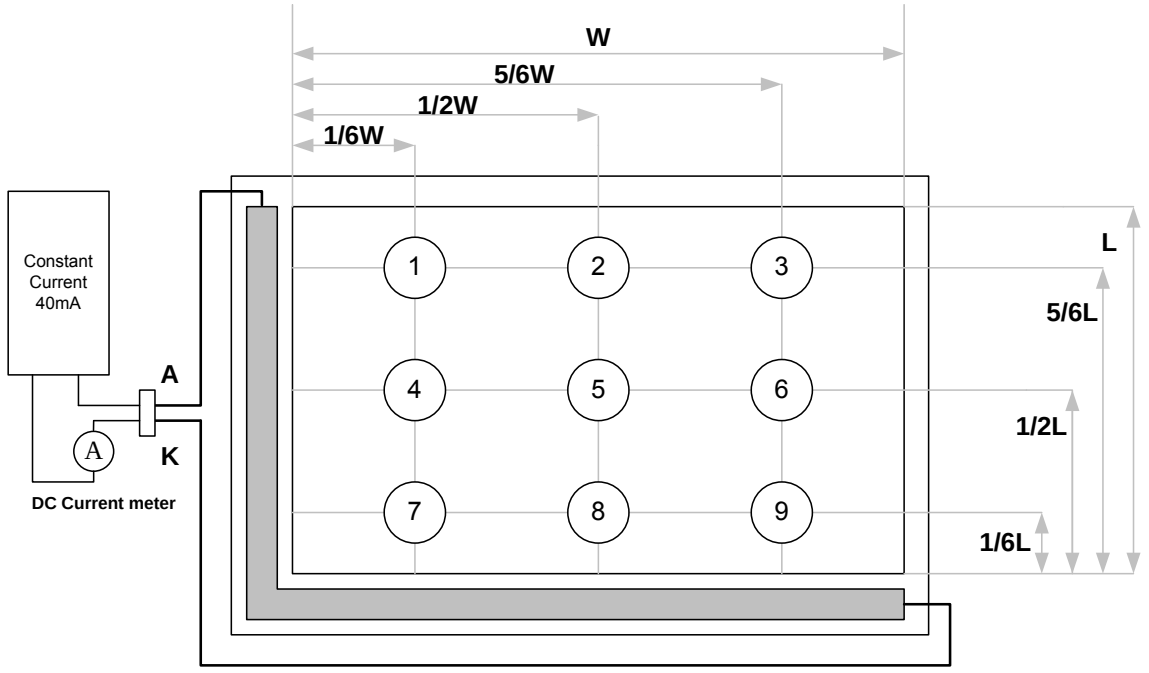
4.2 Optical characteristic of the LED Back-light

ITEM	MIN	TYP	MAX	UNIT	Condition
Bare Brightness	2800	--	--	Cd/m2	I_{LED} =40mA,Ta=25℃
AVG. X of 1931 C.I.E.	0.26	0.30	0.34	--	I_{LED} =40mA,Ta=25℃
AVG. Y of 1931 C.I.E.	0.27	0.31	0.35	--	I_{LED} =40mA,Ta=25℃
Brightness Uniformity	75	--	--	%	I_{LED} =40mA,Ta=25℃

( )For reference only. These data should be update according the prototype.

Note1 : Measurement after 10 minutes from LED BL operating.

Note2 : Measurement of the following 9 places on the display.



Note3: The Uniformity definition

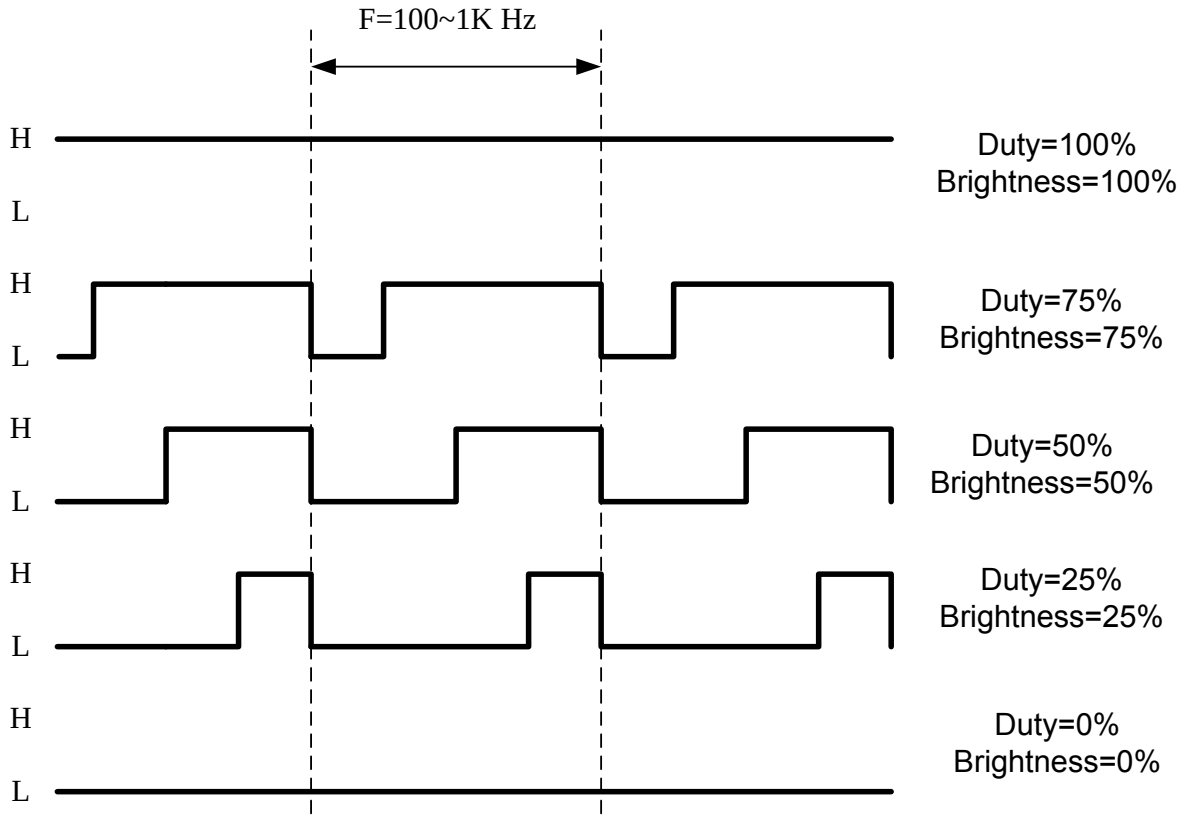
(Min Brightness / Max Brightness) x 100%

5 Interface specifications

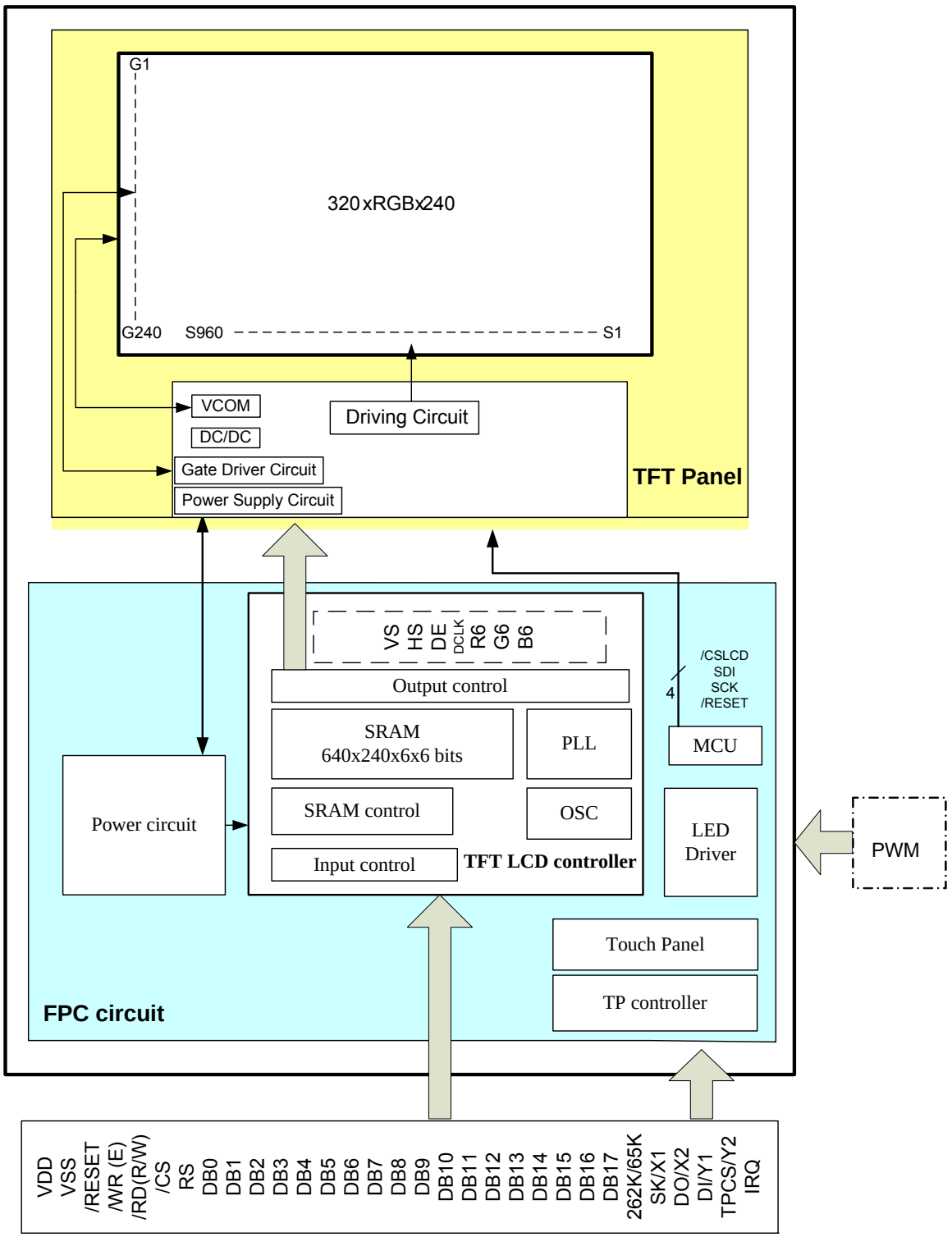
Pin no	Symbol	I/O	Description	Remark
1	DGND	-	GND	
2				
3	PWM	-	LED dimming control(with LED driver IC).	
4	NC	-	Must be floating.	
5	/RESET	I	Reset signal for TFT LCD controller.	
6	RS	I	Register and Data select for TFT LCD controller.	
7	/CS506	I	Chip select low active signal for TFT LCD controller.	
8	/WR	I	80mode: /WR low active signal for TFT LCD controller. 68mode: E signal latch on rising edge.	
9	/RD	I	80mode: /RD low active signal for TFT LCD controller. 68mode: R/W signal Hi: read, Lo: write.	
10	DB0	I	Data bus.	
11	DB1	I		
12	DB2	I		
13	DB3	I		
14	DB4	I		
15	DB5	I		
16	DB6	I		
17	DB7	I		
18	DB8	I		
19	DB9	I		
20	DB10	I		
21	DB11	I		
22	DB12	I		
23	DB13	I		
24	DB14	I		
25	DB15	I		
26	DB16	I		
27	DB17	I		
28	262K/65K	I	Hi=262 K Color Mode; Lo: 65 K Color Mode.	
29	DGND	-	GND	
30	NC	I	No connection	
31	NC	I	No connection	
32	NC	I	No connection	
33	NC	I	No connection	
34	NC	I	No connection	
35-37	VDD	-	Power supply for the logic (3.3V).	
38-40	DGND	-	GND.	

NOTE :
Pin3: PWM signal input. It is for brightness control.

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
ADJ signal frequency	f_{PWM}	100	--	1K	Hz
ADJ signal logic level High	VIH	2.0	--	3.3V	V
ADJ signal logic level Low	VIL	0	--	0.8	V

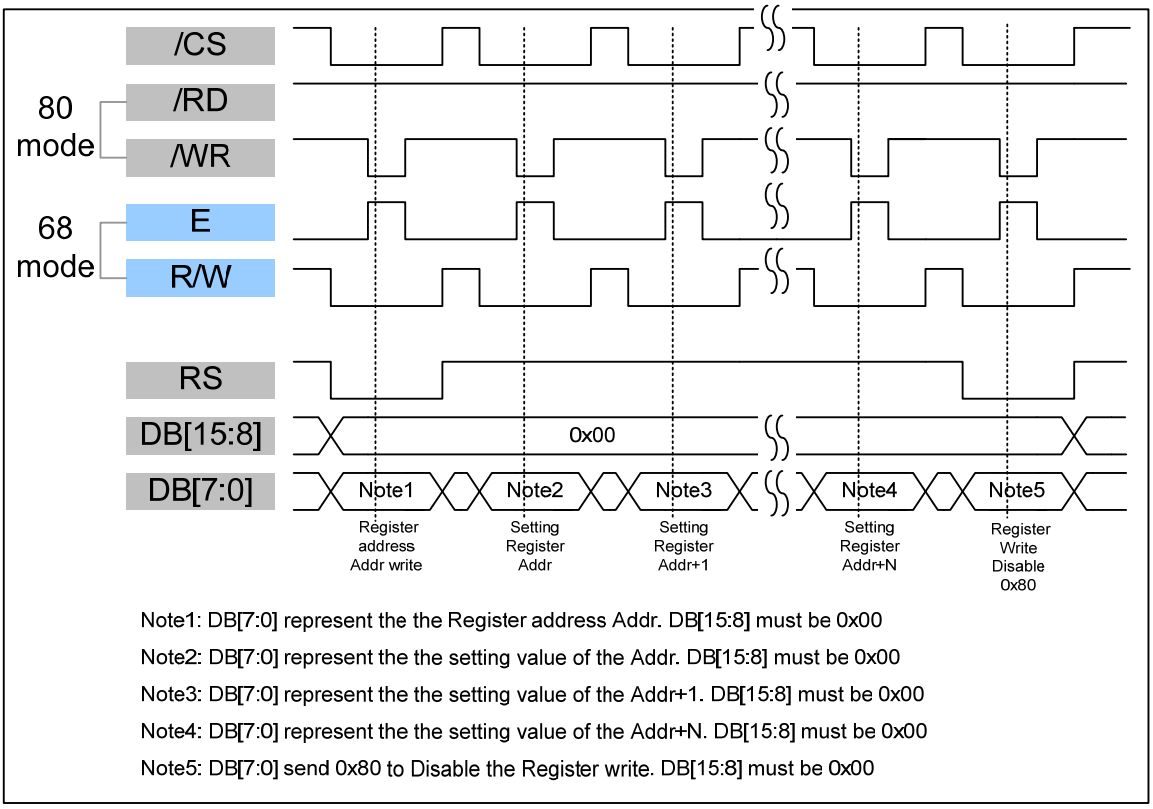


6 BLOCK DIAGRAM



7 Interface Protocol

7.1 16Bit-80/68- Write to Command Register



Note1: DB[7:0] represent the the Register address Addr. DB[15:8] must be 0x00

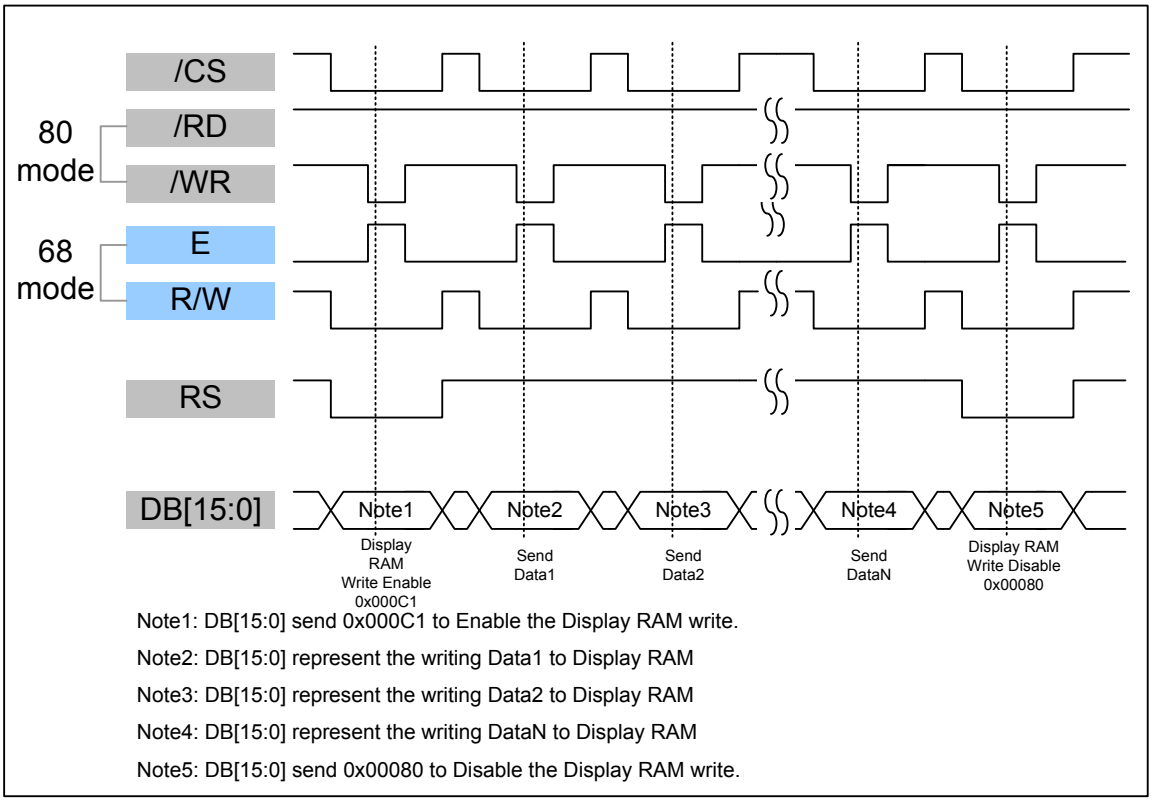
Note2: DB[7:0] represent the the setting value of the Addr. DB[15:8] must be 0x00

Note3: DB[7:0] represent the the setting value of the Addr+1. DB[15:8] must be 0x00

Note4: DB[7:0] represent the the setting value of the Addr+N. DB[15:8] must be 0x00

Note5: DB[7:0] send 0x80 to Disable the Register write. DB[15:8] must be 0x00

7.2 16Bit-80/68-Write to Display RAM



Note1: DB[15:0] send 0x000C1 to Enable the Display RAM write.

Note2: DB[15:0] represent the writing Data1 to Display RAM

Note3: DB[15:0] represent the writing Data2 to Display RAM

Note4: DB[15:0] represent the writing DataN to Display RAM

Note5: DB[15:0] send 0x00080 to Disable the Display RAM write.

7.3 Data transfer order Setting

7.3.1 18 bit interface 262K color only (Pin28 65K/262K =High)

DB	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

7.3.2 16 bit interface 65K color (Pin28 65K/262K =Low)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

7.3.3 16 bit interface 262K color (Pin28 65K/262K =High)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	X	X	X	X	X	X	X	R5	R4
2nd data	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

7.3.4 9 bit interface 262K color only (Pin28 65K/262K =High)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3
2nd data	X	X	X	X	X	X	X	G2	G1	G0	B5	B4	B3	B2	B1	B0

7.3.5 8 bit interface 65K color (Pin28 65K/262K =Low)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3
2nd data	X	X	X	X	X	X	X	X	G2	G1	G0	B4	B3	B2	B1	B0

7.3.6 8 bit interface 262K color (Pin28 65K/262K =High)

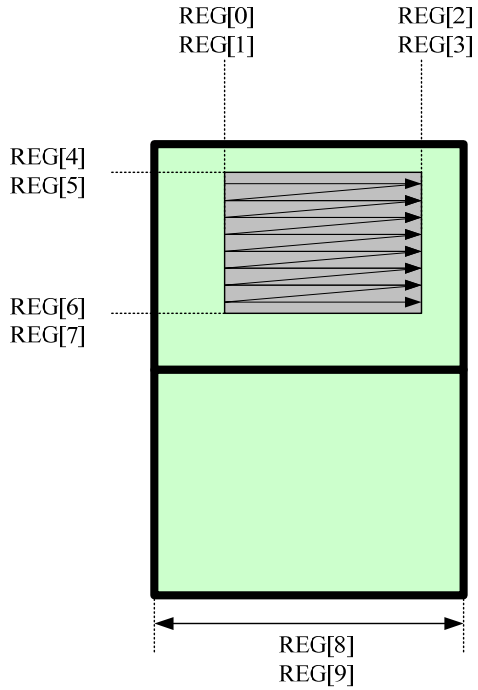
DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	X							R5	R4
2nd data	X	X	X	X	X	X	X	X	R3	R2	R1	R0	G5	G4	G3	G2
3rd data	X	X	X	X	X	X	X	X	G1	G0	B5	B4	B3	B2	B1	B0

8 Register Depiction

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
00	00	MSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
01	00	LSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
02	01	MSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
03	3F	LSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
04	00	MSB of Y-axis start position								
Description	set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
05	00	LSB of Y-axis start position								
Description	Set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
06	00	MSB of Y-axis end position								
Description	set the vertical end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
07	EF	LSB of Y-axis end position								
Description	Set the vertical end position of display active region									

To simplify the address control of display RAM access, the window area address function
allows for writing data only within a window area of display RAM specified by registers REG[00]~REG[07] .
After writing data to the display RAM, the Address counter will be increased within setting window address-range which is specified by

MIN X address (REG[0] & REG[1])
MAX X address (REG[2] & REG[3])
MIN Y address (REG[4] & REG[5])
MAX Y address (REG[6] & REG[7])
Therefore, data can be written consecutively without thinking the data address.



Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
08	01	X	X	X	X	X	X	_PanelXSize H_Byte[1:0]		
Description	Set the panel X size									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
09	40	_PanelXSize L_Byte[7:0]								
Description	Set the panel X size									

The register REG[08] and REG[09] is use to calculate the RAM address. If you want to use the TFT as Landscape mode (320x240), the REG[08] & RGE[09 must set to 320. If you want to use the TFT as Portrait mode (240x320), the REG[08] & RGE[09] must set to 240.

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0A	00	X	X	X	X	X	[17:16] bits of memory write start address			
Description	Memory write start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0B	00	[15:8] bits of memory write start address								
Description	Memory write start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0C	00	[7:0] bits of memory write start address								
Description	Memory write start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x10	0x0D	Bit_SWAP	OUT_TEST	BUS_SEL		Blanking	P/S_SEL	CLK_SEL		
Description	"0x10_Clk_sel[1:0]" : The TFT controller built-in 40Mhz PLL clock. These bits are for select the TFT panel dot clock frequency. 00 : 20Mhz 01: 10Mhz 02: 5 Mhz									
	"0x10_ps_sel[2]" : The TFT controller support parallel and serial RGB interface. These bits are for select the output timing. 0 : serial Panel 1: Parallel panel									
	"0x10_blanking_tmp[3]" 0 : OFF (blanking) 1: ON (normal operation)									
	"0x10_bus_sel[5:4]" : It only for serial Panel 00=R , 01=G , 10=B									
	"0x10_out_test[6]" : Self test 0 : normal operation 1: for test (don't use for normal operation) When set the bit to "1" , the Rout=(Reg 2a[6:0]) Gout=(Reg 2b[6:0]) Bout=(Reg 2c[6:0])									
	"0x10_bit_swap[7]" : 0-normal									
	The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x11	00	X	X	EVEN			_ODD			
Description	" Even line of serial panel data out sequence or data bus order of parallel panel 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved									

	Odd line of serial panel data out sequence 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG **101: BGR** Others: reserved **Must Set to 0x05 for AM320240N1**

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x12	00					Hsync_stH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x13	00	Hsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x14	00					Hsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x15	10	Hsync_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x16	00					Hact_stH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x17	38	Hact_stL_Byte[7:0]								
Description	For TFT output timing adjust: DE pulse start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark

(Hex)										
0x18	01					Hact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x19	40	Hact_pwL_Byte[7:0]								
Description	For TFT output timing adjust: DE pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1A	01					HtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync total clocks H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1B	B8	HtotalL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync total clocks H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1C	00					Vsync_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1D	00	Vsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1E	00					Vsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1F	08	Vsync_pwL_Byte[7:0]								

Description	For TFT output timing adjust: Vsync pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x20	00					Vact_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical DE pulse start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x21	12	Vact_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical DE pulse start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x22	00					Vact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical Active width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x23	F0	Vact_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical Active width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x24	01					VtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical total width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x25	09	VtotalL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical total width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it.									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
26	00	X	X	X	X	X	[17:16] bits of memory read start			

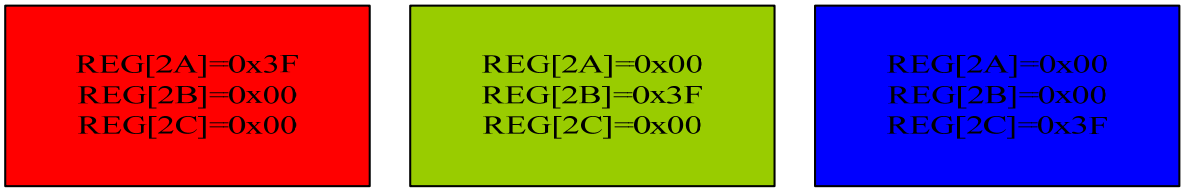
							address			
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
27	00	[15:8] bits of memory write start address								
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
28	00	[7:0] bits of memory write start address								
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
29	00	[7:1] Reversed								
Description	[0] Load output timing related setting (H sync., V sync. and DE) to take effect									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2A	00	X	TestPatternRout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Rout data equal to TestPatternRout[6:0]									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2B	00	X	TestPatternGout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Gout data equal to TestPatternGout[6:0]									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2C	00	X	TestPatternBout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Bout data equal to TestPatternBout[6:0]									

If you set the " REG[0x10]_out_test[6]" : Self test =1 , the TFT controller will skip the connect of the display RAM. The Output port will send the REG[2A] ,REG[2B],REG[2C] data.



Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2D	00	X	X	X	X	[3]	Rising/falling edge[2]	_rotate [1:0]		

Description	[3] Output pin X_DCON level control ; TFT Power ON/OFF control 0: TFT POWER circuit OFF 1: TFT POWER circuit ON									
	Rising/falling edge[2] : 0: The RGB out put data are on the Rising edge of the DCLK. 1: The RGB out put data are on the Falling edge of the DCLK.									
	_rotate [1:0]: 00 : rotate 0 degree 01 : rotate90 degree 10 : rotate 270 degree 11 : rotate 180 degree									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
30	00	X	X	X	X	X	_H byte H-Offset[3:0]			
Description	Set the Horizontal offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
31	00	_L byte H-Offset[7:0]								
Description	Set the Horizontal offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
32	00	X	X	X	X	X	_H byte V-Offset[3:0]			
Description	Set the Vertical offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
33	00	_L byte V-Offset[7:0]								
Description	Set the Vertical offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
34	00	[7:4] Reserved					_H byte H-def[3:0]			
Description	[3:0] MSB of image horizontal physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
35	40	_L byte H-def[7:0]								
Description	[7:0] LSB of image horizontal physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
36	01	[7:4] Reserved					_H byte V-def[3:0]			
Description	[3:0] MSB of image vertical physical resolution in memory									
Register	Default	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark

Address (Hex)	(Hex)									
37	E0	_L byte V-def[7:0]								
Description	[7:0] LSB of image vertical physical resolution in memory									

The total RAM size is 640x240x18bit. The user can arrange the Horizontal ram size by REG[34],REG[35] and the Vertical ram size by REG[36],REG[37].
EX: 320x480x18bit REG[34]=0x01 , REG[35]=0x40 , REG[36]=0x01 , REG[37]=0xE0
EX: 640x240x18bit. REG[34]=0x02 , REG[35]=0x80 , REG[36]=0x00 , REG[37]=0xF0

9 Application Note:

```
/* Exported types ------------------------------------------------------------*/
typedef    unsigned   char        uint8;
typedef    signed     char        int8;
typedef    unsigned   short       uint16;
typedef    signed     short       int16;
typedef    unsigned long          uint32;
typedef    signed     int         int32;


/*****************************************************************/
/*                  STEP1: Define MCU BUS type                   */
/*****************************************************************/
    #define Mode80      // 8080 MCU   /WR   /RD
  //#define Mode68      // 6800 MCU   R/W   E
/*****************************************************************/
/*                  STEP2: Define BUS wide                       */
/*****************************************************************/
  //#define C80_18B
  /#define C80_16B
  //#define C80_9B
  //#define C80_8B
/*****************************************************************/
/*                  STEP3: Define Landscap/Portrait              */
/*****************************************************************/
  #define Landscap
  //#define Portrait
/*****************************************************************/
/*                  STEP4: Define Resolution                     */
/*****************************************************************/
#ifdef Landscap
#define       Resolution_X 320
#define       Resolution_Y 240

#endif

#ifdef Portrait
#define       Resolution_X 240
#define       Resolution_Y 320
#endif
```

```
/*****************************************************************/
/*                    STEP5: TFT timing                          */
/*****************************************************************/

#define Rising                  0<<2        // Don't need to change
#define Falling                 1<<2        // Don't need to change

#define LCD_DCLK                8           // Select DCLK Frequency MHz
                                            // (can be 5,6,7,8,10,12,15)

#define LCD_DCLK_Latch          Rising      // Rising: for Rising Edge
                                            // Falling: for Rising Edge

#define H_Sync_Pluse_Wide       10          // Hsync Pluse Wide
#define H_Sync_to_DE            68          // DE horizontal start position
#define H_Sync_total            408         // Horizontal total
#define V_Sync_Pluse_Wide       8           // Vsync Pluse Wide
#define V_Sync_to_DE            18          // DE vertical start position
#define V_Sync_total            262         // Vertical total


//*****************************************************************//
/**************Don't need to change the bellow macro**************/

#if LCD_DCLK== 5
   #define R41          1
   #define R42          1
   #define R10_B10      2
#endif

#if LCD_DCLK== 6
   #define R41          3
   #define R42          4
   #define R10_B10      2
#endif

#if LCD_DCLK== 7
   #define R41          4
   #define R42          3
   #define R10_B10      1
#endif
```

```
#if LCD_DCLK== 8
   #define R41          12
   #define R42          10
   #define R10_B10   1
#endif

#if LCD_DCLK== 10
   #define R41          1
   #define R42          1
   #define R10_B10   1
#endif

#if LCD_DCLK== 12
   #define R41          5
   #define R42          6
   #define R10_B10   1
#endif


#if LCD_DCLK== 15
   #define R41          2
   #define R42          3
   #define R10_B10   1
#endif


#define _DisplayRAM_WriteEnable_ 0xc1
#define _DisplayRAM_WriteDisable_ 0x80


typedef struct
{
      uint8   REG_Index;
      uint8   REG_Value;

}FSA506_REG_Setting;

#ifdef   Landscap
```

```
static    FSA506_REG_Setting FSA506_A[] =

{
  {0x40,0x12},
  {0x41,R41},
  {0x42,R42},
  {0x08,(uint8)(Resolution_X>>8)},
  {0x09,(uint8)(Resolution_X)},
  {0x0a,0x00},
  {0x0b,0x00},
  {0x0c,0x00},
  {0x10,0x0C|R10_B10},
  //{0x10,0x0C|0x02},
  {0x11,0x05},
  {0x12,0x00},
  {0x13,0x00},
  {0x14,(uint8)(H_Sync_Pluse_Wide>>8)},
  {0x15,(uint8)(H_Sync_Pluse_Wide)},
  {0x16,(uint8)(H_Sync_to_DE>>8)},
  {0x17,(uint8)(H_Sync_to_DE)},
  {0x18,(uint8)(Resolution_X>>8)},
  {0x19,(uint8)(Resolution_X)},
  {0x1a,(uint8)(H_Sync_total>>8)},
  {0x1b,(uint8)(H_Sync_total)},
  {0x1c,0x00},
  {0x1d,0x00},
  {0x1e,(uint8)(V_Sync_Pluse_Wide>>8)},
  {0x1f,(uint8)(V_Sync_Pluse_Wide)},
  {0x20,(uint8)(V_Sync_to_DE>>8)},
  {0x21,(uint8)(V_Sync_to_DE)},
  {0x22,(uint8)(Resolution_Y>>8)},
  {0x23,(uint8)(Resolution_Y)},
  {0x24,(uint8)(V_Sync_total>>8)},
  {0x25,(uint8)(V_Sync_total)},
  {0x26,0x00},
  {0x27,0x00},
  {0x28,0x00},
  {0x29,0x01},
```

```
  {0x2d,LCD_DCLK_Latch|0x08},
  // [7:4] Reserved
  // [3] Output pin X_DCON level control
  // [2] Output clock inversion        0: Normal 1: Inverse
  // [1:0] Image rotate
//        00: 0°    01: 90°    10: 270° 11: 180°

  {0x30,0x00},
  {0x31,0x00},
  {0x32,0x00},
  {0x33,0x00},
  {0x34,(uint8)(Resolution_X>>8)},
  {0x35,(uint8)(Resolution_X)},
  {0x36,(uint8)((2*Resolution_Y)>>8)},
  {0x37,(uint8)(2*Resolution_Y)},

};
#endif

#ifdef    Portrait

static    FSA506_REG_Setting FSA506_A[] =

{
  {0x40,0x12},
  {0x41,R41},
  {0x42,R42},
  {0x08,(uint8)(Resolution_X>>8)},
  {0x09,(uint8)(Resolution_X)},
  {0x0a,0x00},
  {0x0b,0x00},
  {0x0c,0x00},
  {0x10,0x0C|R10_B10},
  //{0x10,0x0C|0x02},
  {0x11,0x05},
  {0x12,0x00},
  {0x13,0x00},
  {0x14,(uint8)(H_Sync_Pluse_Wide>>8)},
  {0x15,(uint8)(H_Sync_Pluse_Wide)},
  {0x16,(uint8)(H_Sync_to_DE>>8)},
  {0x17,(uint8)(H_Sync_to_DE)},
```

```
  {0x18,(uint8)(Resolution_Y>>8)},
  {0x19,(uint8)(Resolution_Y)},
  {0x1a,(uint8)(H_Sync_total>>8)},
  {0x1b,(uint8)(H_Sync_total)},
  {0x1c,0x00},
  {0x1d,0x00},
  {0x1e,(uint8)(V_Sync_Pluse_Wide>>8)},
  {0x1f,(uint8)(V_Sync_Pluse_Wide)},
  {0x20,(uint8)(V_Sync_to_DE>>8)},
  {0x21,(uint8)(V_Sync_to_DE)},
  {0x22,(uint8)(Resolution_X>>8)},
  {0x23,(uint8)(Resolution_X)},
  {0x24,(uint8)(V_Sync_total>>8)},
  {0x25,(uint8)(V_Sync_total)},
  {0x26,0x00},
  {0x27,0x00},
  {0x28,0x00},
  {0x29,0x01},


  {0x2d,LCD_DCLK_Latch|0x08|0x01},
  // [7:4] Reserved
  // [3] Output pin X_DCON level control
  // [2] Output clock inversion        0: Normal 1: Inverse
  // [1:0] Image rotate
//        00: 0°    01: 90°    10: 270° 11: 180°

  {0x30,0x00},
  {0x31,0x00},
  {0x32,0x00},
  {0x33,0x00},
  {0x34,(uint8)(Resolution_X>>8)},
  {0x35,(uint8)(Resolution_X)},
  {0x36,(uint8)((2*Resolution_Y)>>8)},
  {0x37,(uint8)(2*Resolution_Y)},

};
#define             NOP()             __asm{NOP}

#endif
```

```
/**************Don't need to change the above macro**************/

void AMP506_80Mode_Command_SendAddress(uint8 Addr);
void AMP506_80Mode_Command_SendData(uint8 Data);
void AMP506_80Mode_16Bit_Memory_SendData(uint16 Dat16bit);
void AMP506_Command_Write(uint8 CMD_Address,uint8 CMD_Value);
void Initial_AMP506(void) ;
void AMP506_WindowSet(uint16 S_X,uint16 S_Y,uint16 E_X,uint16 E_Y)    ;
void FD506_DisplayRAM_WriteEnable(void);
void FD506_DisplayRAM_WriteDisable(void);
void GUI_RectangleFill(uint32 x0, uint32 y0, uint32 x1, uint32 y1, uint16 color);
void Full_LCD(uint16 Dat16bit);

/**************FSA506 Write Registr Address function    ************************/
void AMP506_80Mode_Command_SendAddress(uint8 Addr)
{

   #ifdef Mode68
   uint16 i;
   CLR_nWRL;
   CLR_RS;
   CLR_CS1;
   CLR_nRD;
   DB16OUT(Addr);
   NOP();NOP();
   SET_nWRL;      //Enable
   NOP();NOP();NOP();    NOP();NOP();//NOP(); NOP();NOP();NOP();
   CLR_nWRL;      //Enable
   SET_RS;

   SET_CS1;
   #endif



   #ifdef Mode80
   SET_nRD;                    //SET_RW
   CLR_RS;
   DB16OUT(Addr); NOP();
   CLR_CS1;
   CLR_nWRL;                   //CLR_E
```

```
    NOP();NOP();NOP();
    SET_nWRL;                   //SER_E          // Low to High Latch Data to AMP506 Buffer
    SET_RS;
    SET_CS1;
    #endif


}
/**************FSA506 Write Command Data function    ************************/
void AMP506_80Mode_Command_SendData(uint8 Data)
{
    #ifdef Mode68
    uint16 i;
    CLR_nWRL;      //E
    SET_RS;
    CLR_CS1;
    CLR_nRD;        //W/R
    DB16OUT(Data);
    NOP();NOP();
    SET_nWRL;
    NOP();NOP();NOP();NOP();NOP();//NOP();NOP();NOP();
    CLR_nWRL;      //E nable
    SET_RS;
    SET_CS1;

    #endif

    #ifdef Mode80
    SET_nRD;
    SET_RS;
    DB16OUT(Data); NOP(); // NOP()
    CLR_CS1;
    CLR_nWRL;

    NOP();NOP();NOP();
    SET_nWRL;                           // Low to High Latch Data to AMP506 Buffer
    SET_RS;
    SET_CS1;
    #endif
```

```
}
/**************FSA506 Write Data function    ************************/
void AMP506_80Mode_16Bit_Memory_SendData(uint16 Dat16bit)
{


 #ifdef Mode80
  #ifdef C80_16B
  SET_nRD;
  SET_RS;
  DB16OUT(Dat16bit);NOP();
  CLR_CS1;

  CLR_nWRL;

  NOP(); NOP();    NOP();

  SET_nWRL;                              // Low to High Latch Data to AMP506 Buffer
  SET_CS1;

  #endif

  #ifdef C80_8B
  DB16OUT(Dat16bit>>8);NOP();NOP();
  SET_nRD;
  SET_RS;

  CLR_CS1;
  CLR_nWRL;

  NOP(); NOP();    NOP();
  SET_nWRL;                              // Low to High Latch Data to AMP506 Buffer
  SET_CS1;

  //Delay_uS(1);
  DB16OUT(Dat16bit);NOP(); NOP();
  SET_nRD;
  SET_RS;

  CLR_CS1;
  CLR_nWRL;
```

```
NOP(); NOP();    NOP();
SET_nWRL;                          // Low to High Latch Data to AMP506 Buffer
SET_CS1;

#endif
//Delay_uS(1);


#ifdef C80_18B

uint32 k=0;
uint16 R_temp,G_temp,B_temp;

R_temp=((0xf800&Dat16bit)>>11);
G_temp=((0x07e0&Dat16bit)>>5);
B_temp=((0x001f&Dat16bit));

k|=((R_temp<<1)<<12);    //+G_temp+B_temp;
k|=(G_temp<<6);
k|=(B_temp<<1);

FIO1MASK=0xFFE0FFFF;                        // FIOMASK 只可寫 P1.20~P1.16
FIO1PIN=k;                        // 將 Address A20~A16 寫入 P1.20~P1.16
FIO1MASK=0x00;


SET_nRD;
SET_RS;
DB16OUT(k);NOP();
CLR_CS1;
CLR_nWRL;

 NOP(); NOP();    NOP();


SET_nWRL;                          // Low to High Latch Data to AMP506 Buffer
SET_CS1;

#endif
```

```
  #ifdef C80_9B

  uint32 k=0;
  uint16 R_temp,G_temp,B_temp;

  R_temp=((0xf800&Dat16bit)>>11);
  G_temp=((0x07e0&Dat16bit)>>5);
  B_temp=((0x001f&Dat16bit));

  k|=((R_temp<<1)<<12);    //+G_temp+B_temp;
  k|=(G_temp<<6);
  k|=(B_temp<<1);



  SET_nRD;
  SET_RS;
  CLR_CS1;
  CLR_nWRL;

  DB16OUT(((k&0x3FE00)>>9));

  SET_nWRL;                          // Low to High Latch Data to AMP506 Buffer
  DB16OUT((k&0x1FF)); NOP();
  SET_CS1;
 // Delay_uS(1);
  SET_nRD;
  SET_RS;
  CLR_CS1;
  CLR_nWRL;

  NOP(); NOP();    NOP();

  SET_nWRL;                          // Low to High Latch Data to AMP506 Buffer
  SET_CS1;

  #endif
 #endif
```

```
#ifdef Mode68
  #ifdef C80_16B
  uint16 i;
  NOP();NOP();

  CLR_nWRL;   //E=0
  SET_RS;
  CLR_CS1;
  CLR_nRD;    // W/R=0

  DB16OUT(Dat16bit);

  SET_nWRL;                       // Low to High Latch Data to AMP506 Buffer
  NOP();NOP();NOP();NOP();//NOP();NOP();NOP();NOP();
  CLR_nWRL;                       // Low to High Latch Data to AMP506 Buffer
  SET_CS1;
  #endif


  #ifdef C80_8B
  uint16 i;
  //for (i=0;i<16;i++);
  NOP();NOP();
  CLR_nWRL;   //E=0
  SET_RS;
  CLR_CS1;
  CLR_nRD;    // W/R=0

  DB16OUT(Dat16bit>>8);

  SET_nWRL;                       // Low to High Latch Data to AMP506 Buffer
  NOP();NOP();NOP();NOP();//NOP();NOP();NOP();NOP();
  CLR_nWRL;                       // Low to High Latch Data to AMP506 Buffer
  SET_CS1;

  CLR_nWRL;   //E=0
  SET_RS;
  CLR_CS1;
  CLR_nRD;    // W/R=0
```

```
DB16OUT(Dat16bit);

SET_nWRL;                          // Low to High Latch Data to AMP506 Buffer
NOP();NOP();NOP();NOP();//NOP();NOP();NOP();NOP();
CLR_nWRL;                          // Low to High Latch Data to AMP506 Buffer
SET_CS1;

#endif
//Delay_uS(1);


#ifdef C80_18B

uint32 k=0;
uint16 R_temp,G_temp,B_temp;
uint16 i;
NOP();NOP();

R_temp=((0xf800&Dat16bit)>>11);
G_temp=((0x07e0&Dat16bit)>>5);
B_temp=((0x001f&Dat16bit));

k|=((R_temp<<1)<<12);   //+G_temp+B_temp;
k|=(G_temp<<6);
k|=(B_temp<<1);

FIO1MASK=0xFFE0FFFF;                    // FIOMASK 只可寫 P1.20~P1.16
FIO1PIN=k;                  // 將 Address A20~A16 寫入 P1.20~P1.16
FIO1MASK=0x00;


CLR_nWRL;   //E=0
SET_RS;
CLR_CS1;
CLR_nRD;     // W/R=0

DB16OUT(k);

SET_nWRL;                          // Low to High Latch Data to AMP506 Buffer
NOP();NOP();NOP();NOP();NOP();//NOP();NOP();NOP();
CLR_nWRL;                          // Low to High Latch Data to AMP506 Buffer
```

```
SET_CS1;

#endif

#ifdef C80_9B

uint32 k=0;
uint16 R_temp,G_temp,B_temp;
uint16 i;
//for (i=0;i<16;i++);
NOP();NOP();
R_temp=((0xf800&Dat16bit)>>11);
G_temp=((0x07e0&Dat16bit)>>5);
B_temp=((0x001f&Dat16bit));

k|=((R_temp<<1)<<12);    //+G_temp+B_temp;
k|=(G_temp<<6);
k|=(B_temp<<1);



CLR_nWRL;    //E=0
SET_RS;
CLR_CS1;
CLR_nRD;      // W/R=0

DB16OUT(((k&0x3FE00)>>9));

SET_nWRL;                          // Low to High Latch Data to AMP506 Buffer
NOP();NOP();NOP();NOP();//NOP();NOP();NOP();NOP();
CLR_nWRL;                          // Low to High Latch Data to AMP506 Buffer
SET_CS1;

// Delay_uS(1);
CLR_nWRL;    //E=0
SET_RS;
CLR_CS1;
CLR_nRD;      // W/R=0

DB16OUT((k&0x1FF));
```

```
   SET_nWRL;                              // Low to High Latch Data to AMP506 Buffer
   NOP();NOP();NOP();NOP();//NOP();NOP();NOP();NOP();
   CLR_nWRL;                              // Low to High Latch Data to AMP506 Buffer
   SET_CS1;

   #endif
  #endif


}

/**************FSA506 Write Command function    ************************/
void AMP506_Command_Write(uint8 CMD_Address,uint8 CMD_Value)
{
   AMP506_80Mode_Command_SendAddress(CMD_Address);
   AMP506_80Mode_Command_SendData(CMD_Value);
}


/**************FSA506 Initial function    ************************/

void Initial_AMP506(void)               //

{           uint8 i;


       for(i=0;i < (sizeof(FSA506_A) / sizeof (FSA506_A[0]));i++)

       {

          AMP506_Command_Write(FSA506_A[i].REG_Index , FSA506_A[i].REG_Value);

       }

}

/**************FSA506 Set Start & End area function    ************************/
void AMP506_WindowSet(uint16 S_X,uint16 S_Y,uint16 E_X,uint16 E_Y)

{
```

```
        AMP506_80Mode_Command_SendAddress(0x00);

        AMP506_80Mode_Command_SendData((S_X)>>8);
        AMP506_80Mode_Command_SendData(S_X);

        AMP506_80Mode_Command_SendData((E_X-1)>>8);
        AMP506_80Mode_Command_SendData(E_X-1);

        AMP506_80Mode_Command_SendData(S_Y>>8);
        AMP506_80Mode_Command_SendData(S_Y);

        AMP506_80Mode_Command_SendData((E_Y-1)>>8);
        AMP506_80Mode_Command_SendData(E_Y-1);

}

//*****************************************************************************
//                      Enable Display RAM Write
//*****************************************************************************

void FD506_DisplayRAM_WriteEnable(void)
{

    AMP506_80Mode_Command_SendAddress(_DisplayRAM_WriteEnable_);

}

//*****************************************************************************
//                      Disable Display RAM Write
//*****************************************************************************

void FD506_DisplayRAM_WriteDisable(void)
{
    AMP506_80Mode_Command_SendAddress(_DisplayRAM_WriteDisable_);
}

/**************FSA506 Set Start & End area function    ************************/
void GUI_RectangleFill(uint32 x0, uint32 y0, uint32 x1, uint32 y1, uint16 color)
{
    uint32 k,l;
```

```
   AMP506_WindowSet(x0,y0,x1,y1);
   FD506_DisplayRAM_WriteEnable();
  for(k=y0;k<y1;k++)

    {
      for(l=x0;l<x1;l++)
       {
              AMP506_80Mode_16Bit_Memory_SendData(color);
           }
    }
   FD506_DisplayRAM_WriteDisable();

}
/**************Full Display function    ************************/
void Full_LCD(uint16 Dat16bit)
{
   GUI_RectangleFill(0,0,Resolution_X,Resolution_Y,Dat16bit);
}

void main(void)
{

       Initial_AMP506();
       Full_LCD(0xf800);
       Full_LCD(0x07e0);
       Full_LCD(0x001f);

}
```

The TFT LCD controller default value is for AM320240N1 already. So we can start to write our data in a few steps:

Target: To write a 640x240 data to Display RAM and scroll the display data by change the Horizontal offset register.

9.1 Step 1: Make sure the interface Protocol.

9.2 Step 2: Define the Horizontal ram seize = 640 and Vertical ram size =240

640x240x18bit. REG[34]=0x02 , REG[35]=0x80 , REG[36]=0x00 , REG[37]=0xF0

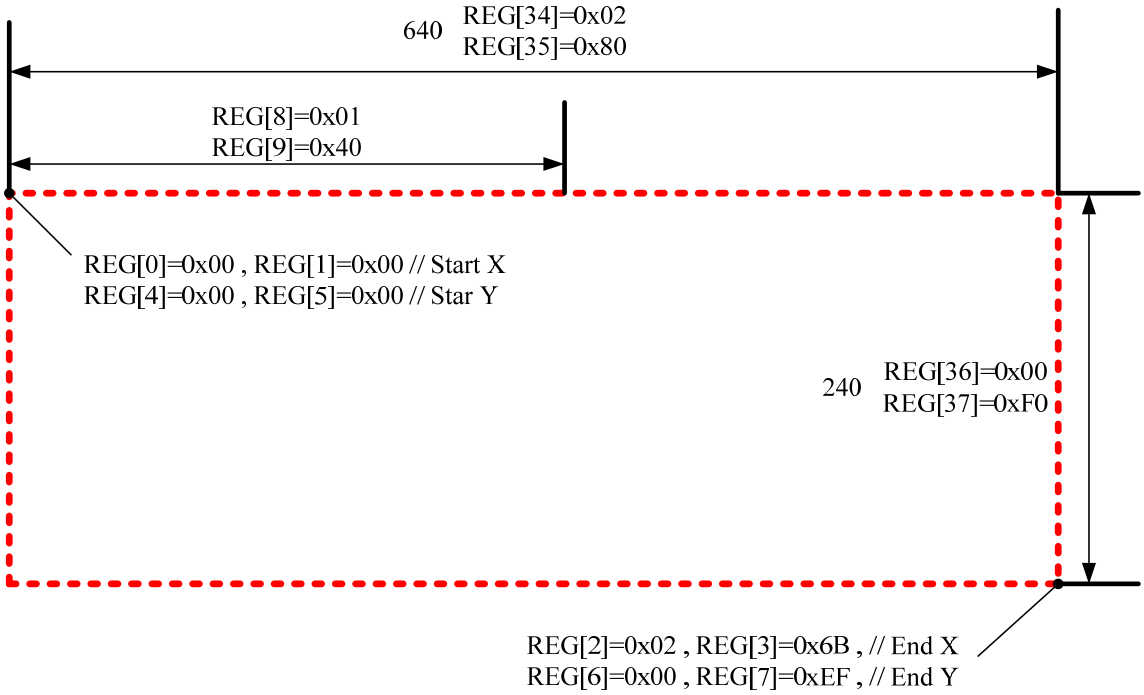
9.3 Step 3: Define the Panel X Size = 320

REG[8]=0x01 , REG[9]=0x40

9.4 Step4: Define the Write window. Start=(0,0) End=(619,239)

REG[0]=0x00 , REG[1]=0x00 , REG[2]=0x02 , REG[3]=0x6B , // Start X , End X

REG[4]=0x00 , REG[5]=0x00 , REG[6]=0x00 , REG[7]=0xEF , // Star Y ,End Y



9.5 Step5: Write the 640x240x18 bit data consecutively

9.6 Step6: The display will show the following image.

9.7 Step7: Change the Horizontal offset to switch or scroll the display data.

Set the Horizontal offset = 160 , REG[30]=00 REG[31]=A0 . You will see

9.8 Step8: Change the Horizontal offset to switch or scroll the display data.

Set the Horizontal offset = 320 , REG[30]=01 REG[31]=40 . You will see

DISPLAYED COLOR AND INPUT DATA

	Color & Gray Scale	DATA SIGNAL																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(31)	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(61)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(31)	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(1)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(31)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

10 QUALITY AND RELIABILITY

1. Scope

Specifications contain

1.1 Display Quality Evaluation

1.2 Mechanics Specification

2. Sampling Plan

Unless there is other agreement, the sampling plan for incoming inspection shall

follow MIL-STD-105E LEVEL II.

2.1 Lot size: Quantity per shipment as one lot (different model as different lot).

2.2 Sampling type: Normal inspection, single sampling.

2.3 Sampling level: Level II.

2.4 AQL: Acceptable Quality Level

Major defect: AQL=0.65

Minor defect: AQL=1.0

3. Panel Inspection Condition

3.1 Environment:

Room Temperature: 25±5°C.

Humidity: 65±5% RH.

Illumination: 300 ~ 700 Lux.

3.2 Inspection Distance:

35-40 cm

3.3 Inspection Angle:

The vision of inspector should be perpendicular to the surface of the Module.

3.4 Inspection time :

Perceptibility Test Time: 20 seconds max.

4. Display Quality

4.1 Function Related:

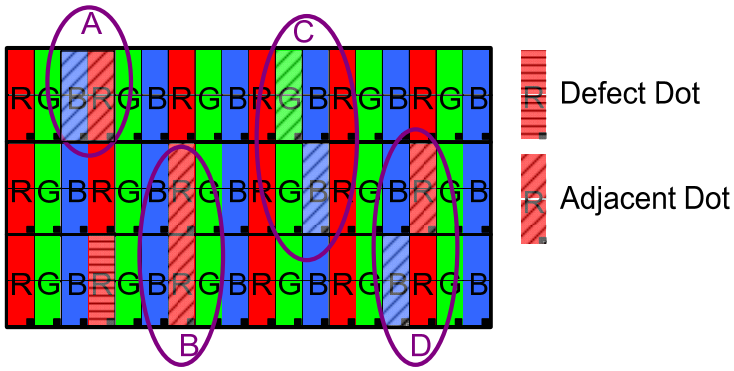
The function defects of line defect, abnormal display, and no display are considered Major defects.

4.2 Bright/Dark Dots:

Defect Type / Specification	G0 Grade	A Grade
Bright Dots	0	N≤ 1
Dark Dots	0	N≤ 3
Total Bright and Dark Dots	0	N≤ 3

[Note 1]

Judge defect dot and adjacent dot as following.



(1) One pixel consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot)

(2) The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.

(3) Allow above (as A, B, C and D status) adjacent defect dots, including bright and dart adjacent dot. And they will be counted 2 defect dots in total quantity.

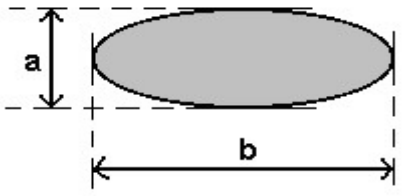
(4) Defects on the Black Matrix, out of Display area, are not considered as a defect or counted.

(5) There should be no distinct non-uniformity visible through 6% ND Filter within 2 sec inspection times.

4.3 Visual Inspection specifications:

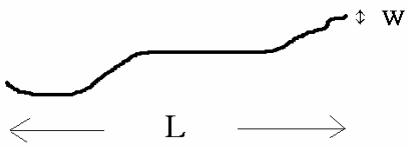
Defect Type	Specification	Count(N)
Dot Shape (Particle、Scratch and Bubbles in display area)	D≤0.15mm	Ignored
	0.15mm < D≤ 0.3mm	N≤ 3
	D > 0.3mm	N=0
Line Shape (Particles、Scratch、Lint and Bubbles in display area)	W≤ 0.05mm	Ignored
	0.05mm<W≤ 0.1mm , L≤ 3mm	N≤ 3
	W > 0.1mm , L > 3mm	N=0

[Note 2] W : Width[mm], L : Length[mm], N : Number, φ : Average Diameter



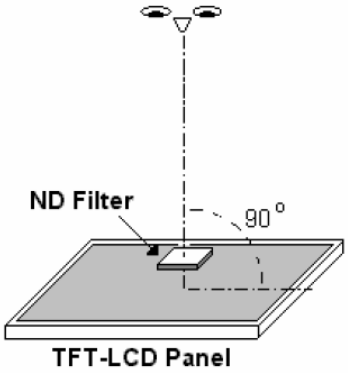
$\phi = (a + b) / 2$

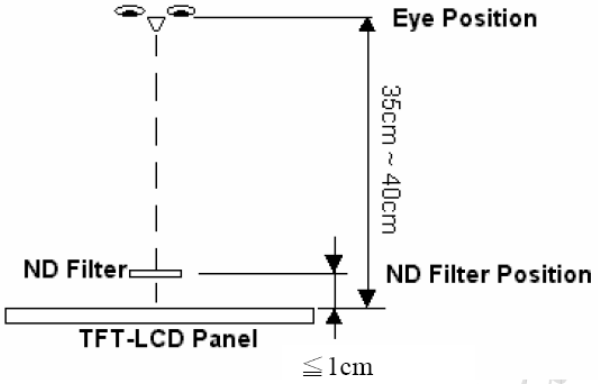
1. (White, black) Spot
2. Polarizer Bubble



1. fiber

[Note 3] Bright dot is defined through 6% transmission ND Filter as following.





11 Reliability test items :

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

12 USE PRECAUTIONS

12.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

12.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

12.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.

3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

12.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

12.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

13 OUTLINE DIMENSION