晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR
LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM-240320MHTNQW-00H
APPROVED BY	
DATE	

☐Approved For Specifications
☐Approved For Specifications & Sample

AMPIRE CO., LTD.
4F., No.116, Sec. 1, Xintai 5th Rd., Xizhi Dist., New Taipei City 221, Taiwan (R.O.C.) 22181 新北市 汐止區新台五路一段 116 號 4F
TEL:886-2-26967269 , FAX:886-2-26967196 or 26967270

APPROVED BY	CHECKED BY	ORGANIZED BY

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2015/01/13	--	New Release	Mark

1 Features

This display module is a color active matrix thin film transistor (TFT) liquid crystal display that uses amorphous silicon TFT as a switching device.
This TFT LCD panel has a 2.8 inch diagonally measured active display area with QVGA resolution (240 horizontal by 320 vertical pixels array).It is suitable for hand-held application. The LCD adopts one backlight with High brightness 4-lamps white LED.

(1) LCD: 1.1 Amorphous-TFT 2.8 inch display, transmissive, normally white type.
1.2 240(RGB) X320 dots Matrix
1.3 LCD Driver IC: ST7789V
1.4 Viewing Direction 12 o'clock (Gray Inversion)
(2) Compatible with ROHS Standard
(3) MCU Interface: SPI interface.
(4) MPU interface: 18bits and 6bits, parallel interface.

2 Mechanical specifications

Item	Specifications	unit
Display resolution(dot)	240(W) x 320(H)	dots
Active area	43.2 (W) x 57.6(H)	mm
Pixel pitch	0.180 (W) x 0.180 (H)	mm
Pixel Arrangement	R.G.B -stripe	-
Overall dimension	50.2 (W) x 98.5(H) x 3.0(D)	mm
Viewing direction	12 o'clock (Gray Inversion)	-
Response Time	16	ms
Contrast ratio	500	-
Display Type	Transmissive	-
Display Mode	Normally White	-

3 Absolute max. ratings and environment

3.1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+4.6	V	-
Logic Power voltage	LED A – LED K	-0.3	+4.0	V	-
Input voltage	VIN	-0.3	VDD+0.5	V	-

3.2 Environment

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	Top	-20	70	℃	-
Storage Temperature	Tst	-30	80	℃	

4 Electrical specifications

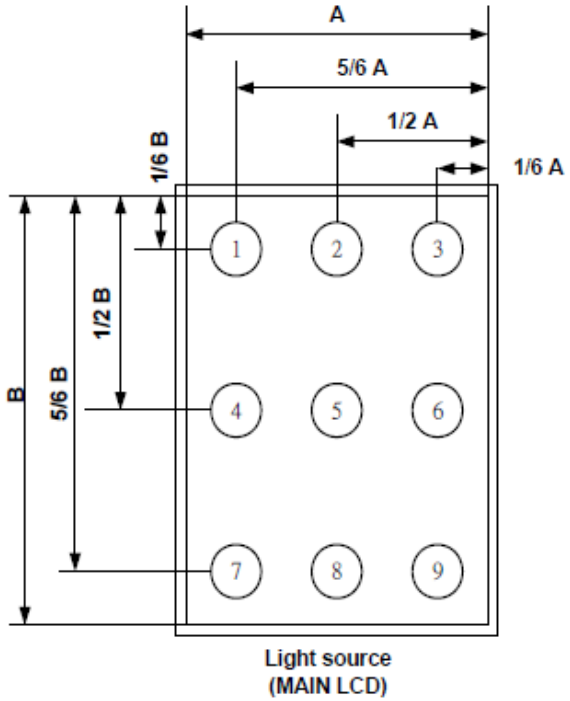
4.1 Electrical characteristics of LCM

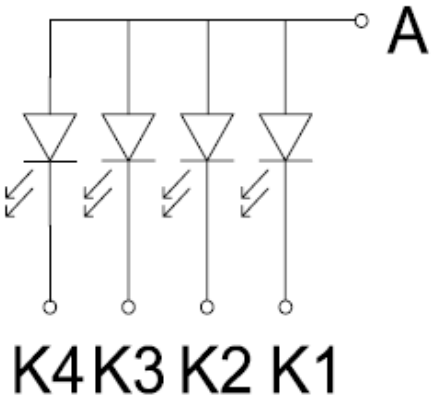
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating voltage	V_{DD}		2.4	2.75	3.3	V
I/O Supply Voltage	V_{DDI}		1.65	1.8	3.3	V
High-level input voltage	V_{IH}		$0.8V_{DDI}$		V_{DDI}	V
Low-level input voltage	V_{IL}		0		$0.2V_{DDI}$	V

4.2 LED back light specification

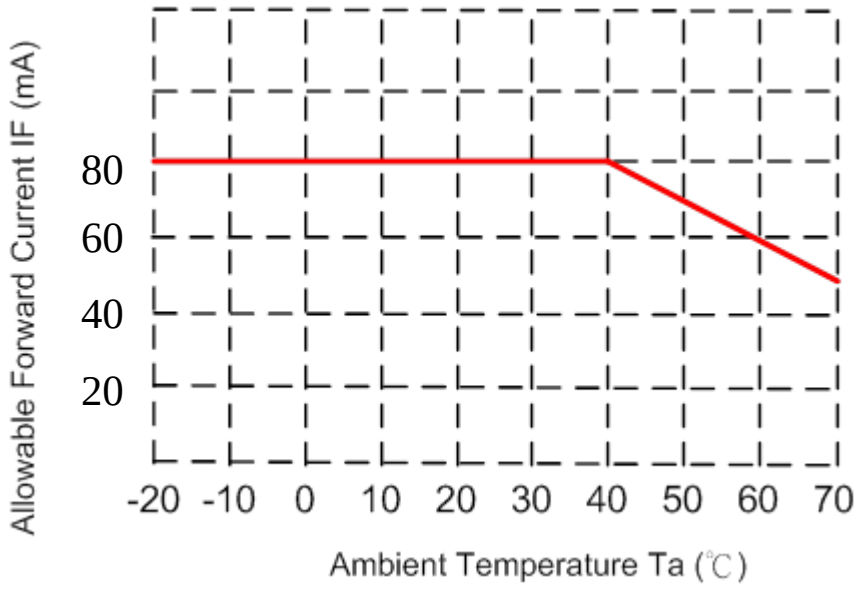
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =80mA	2.8	3.0	3.5	V
Forward current	I_f	4-chip Parallel	-	80	-	mA
Power Consumption	P_{BL}	I_f =80mA	-	288	-	mW
Uniformity (with L/G)	-	I_f=80mA	80%*1	-	-	-
Luminous color	White					
Chip connection	4 chip parallel connection					

Bare LED measure position:





*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 70\%$



5 Optical characteristics

Optical characteristics

Item		Symbol	Conditions	Min	Typ	Max	Unit	Note
Contrast Ratio		CR	Viewing normal angle $\Theta x = \Theta y = 0$	-	500	-	-	
Response Time		T_R+T_F		-	16	-	ms	(4)
Viewing Angle	Top	Θ_T	CR≧10	-	70	-	deg	(2)
	Bottom	Θ_B		-	50	-		
	Left	Θ_L		-	70	-		
	Right	Θ_R		-	70	-		
Module Chromaticity	Red	X_R	Viewing normal angle $\Theta x = \Theta y = 0$	0.576	0.626	0.676	-	-
		Y_R		0.286	0.336	0.386		
	Green	X_G		0.226	0.276	0.326		
		Y_G		0.500	0.550	0.600		
	Blue	X_B		0.094	0.144	0.194		
		Y_B		0.080	0.130	0.180		
	White	X_W		0.257	0.307	0.357		
		Y_W		0.279	0.329	0.379		
Brightness		-	LCD center	200	250	-	Cd/㎡	(1)

Note (1) Measurement Setup:

The LCD module should be stabilized at given temperature(25°C) for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

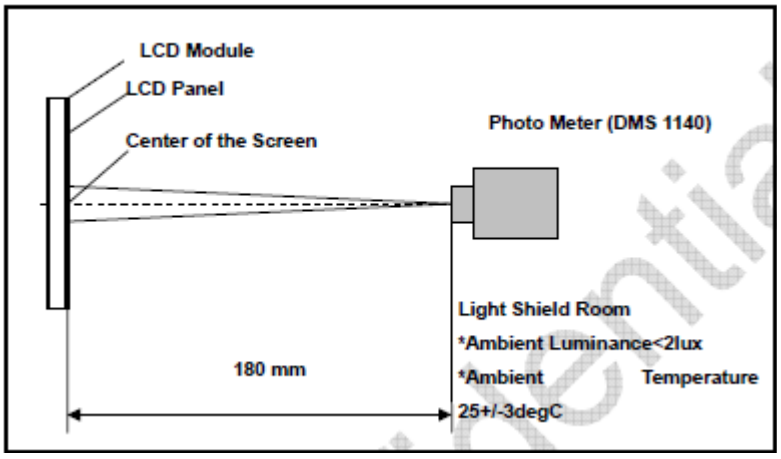


Figure 2 Measurement Setup

Note (2) Definition of Viewing Angle

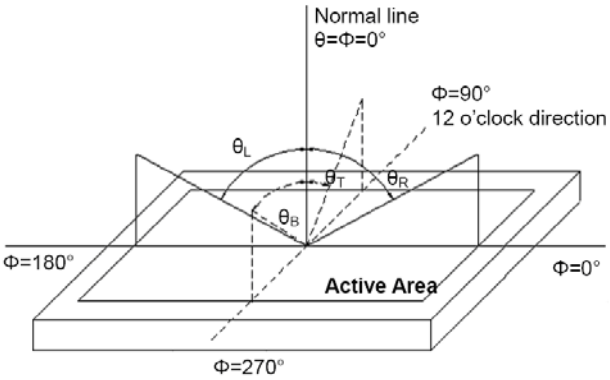


Figure 3 Definition of Viewing Angle

Note (3) Definition Of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (4) Definition Of Response Time

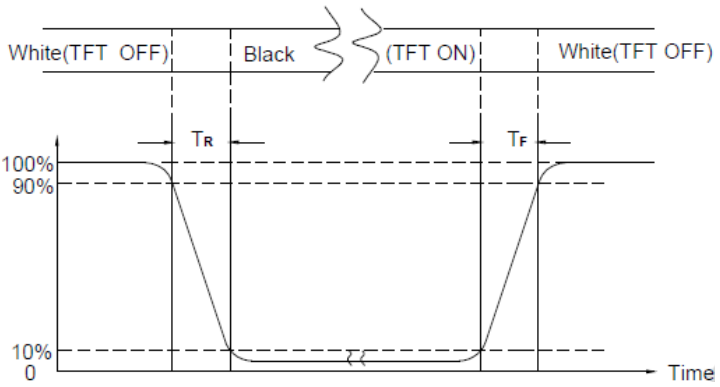


Figure 4 Definition of Response Time

6. Electrical Specifications

6.1 TFT LCD Panel FPC Descriptions

<table>
<tr><th>Pin No.</th><th>Terminal</th><th>Functions</th></tr>
<tr><td>1</td><td rowspan="4">NC</td><td rowspan="4">No Connection.</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td></tr>
<tr><td>4</td></tr>
<tr><td>5</td><td>GND</td><td>GND-terminal.</td></tr>
<tr><td>6</td><td>/CS</td><td>-Chip selection pin
Low enable.
High disable.</td></tr>
<tr><td>7</td><td>WRX</td><td>-Write enable in MCU parallel interface.
- Display data/command selection pin in 4-line serial interface.
- Second Data lane in 2 data lane serial interface.
-If not used, please fix this pin at VDDI or DGND.</td></tr>
<tr><td>8</td><td>DCX/SCL</td><td>-Display data/command selection pin in parallel interface.
-This pin is used to be serial interface clock.
DCX=’1’: display data or parameter.
DCX=’0’: command data.
-If not used, please fix this pin at VDDI or DGND.</td></tr>
<tr><td>9</td><td>RD</td><td>-Read enable in 8080 MCU parallel interface.
-If not used, please fix this pin at VDDI or DGND.</td></tr>
<tr><td>10</td><td>SDI</td><td>-IM3: High, SPI interface input pin.
-The data is latched on the rising edge of the SCL signal.
-If not used, please fix this pin at VDDI or DGND level.</td></tr>
<tr><td>11</td><td>SDO</td><td>Serial bus interface data output pin.
Let SDO as open when not in use.</td></tr>
<tr><td>12</td><td>DB0/PD0</td><td rowspan="18"><table><tr><th>Mode</th><th>DB Pin in use</th></tr><tr><td>Serial Mode/Digital RGB Interface Mode</td><td>SDI, SDO/ PD [17:0]
B[5:0]=PD[5:0]
G[5:0]=PD[11:6]
R[5:0]=PD[17:12]</td></tr></table></td></tr>
<tr><td>13</td><td>DB1/PD1</td></tr>
<tr><td>14</td><td>DB2/PD2</td></tr>
<tr><td>15</td><td>DB3/PD3</td></tr>
<tr><td>16</td><td>DB4/PD4</td></tr>
<tr><td>17</td><td>DB5/PD5</td></tr>
<tr><td>18</td><td>DB6/PD6</td></tr>
<tr><td>19</td><td>DB7/PD7</td></tr>
<tr><td>20</td><td>DB8/PD8</td></tr>
<tr><td>21</td><td>DB9/PD9</td></tr>
<tr><td>22</td><td>DB10/PD10</td></tr>
<tr><td>23</td><td>DB11/PD11</td></tr>
<tr><td>24</td><td>DB12/PD12</td></tr>
<tr><td>25</td><td>DB13/PD13</td></tr>
<tr><td>26</td><td>DB14/PD14</td></tr>
<tr><td>27</td><td>DB15/PD15</td></tr>
<tr><td>28</td><td>DB16/PD16</td></tr>
<tr><td>29</td><td>DB17/PD17</td></tr>
</table>

30	/RESET	-This signal will reset the device and it must be applied to properly initialize the chip. -Signal is active low.
31	ENABLE	-Data enable signal for RGB interface operation. ***-If not used, please fix this pin at VDDI or DGND.***
32	DOTCLK	-Dot clock signal for RGB interface operation. ***-If not used, please fix this pin at VDDI or DGND.***
33	HSYNC	-Horizontal (Line) synchronizing input signal for RGB interface operation. ***- If not used, please fix to VDDI or DGND.***
34	VSYNC	-Vertical (Frame) synchronizing input signal for RGB interface operation. ***-If not used, please fix to the VDDI or DGND.***
35	VDDI	A supply voltage to the internal logic: VDDI = 1.65~3.3V.
36	VDDI	
37	VDD	A supply voltage to the analog circuit. Connect to an external power supply of 2.4 ~ 3.3V.
38	GND	GND-terminal.
39	LED_A	LED Anode.
40	LED_K1	LED Cathode.
41	LED_K2	
42	LED_K3	
43	LED_K4	
44	GND	GND-terminal

6.2 System Function Command Table

(Please refer to ST7789 data sheet)

7 Application

7.1 Power ON/OFF Sequence

VDDI and VDD can be applied in any order.
VDD and VDDI can be power down in any order.
During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec
after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after
RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

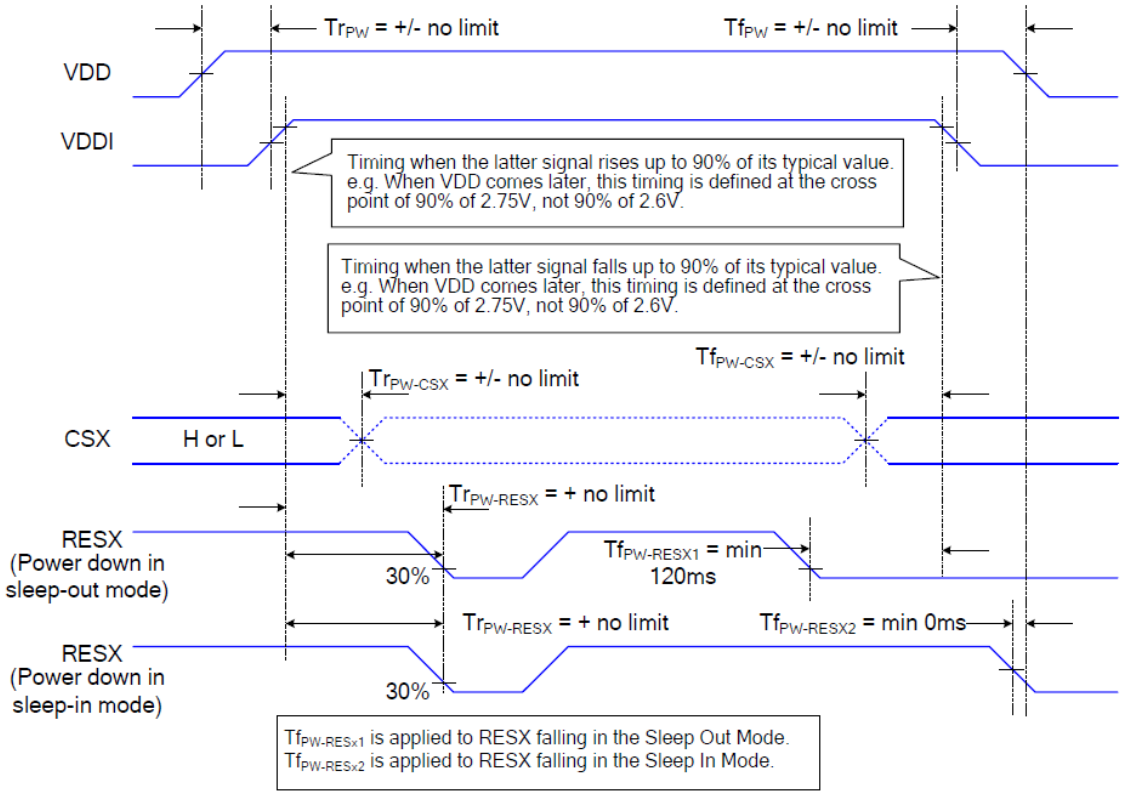
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out
command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to
apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not
guaranteed.

The power on/off sequence is illustrated below



7.1.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

7.2 Power Level Definition

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.

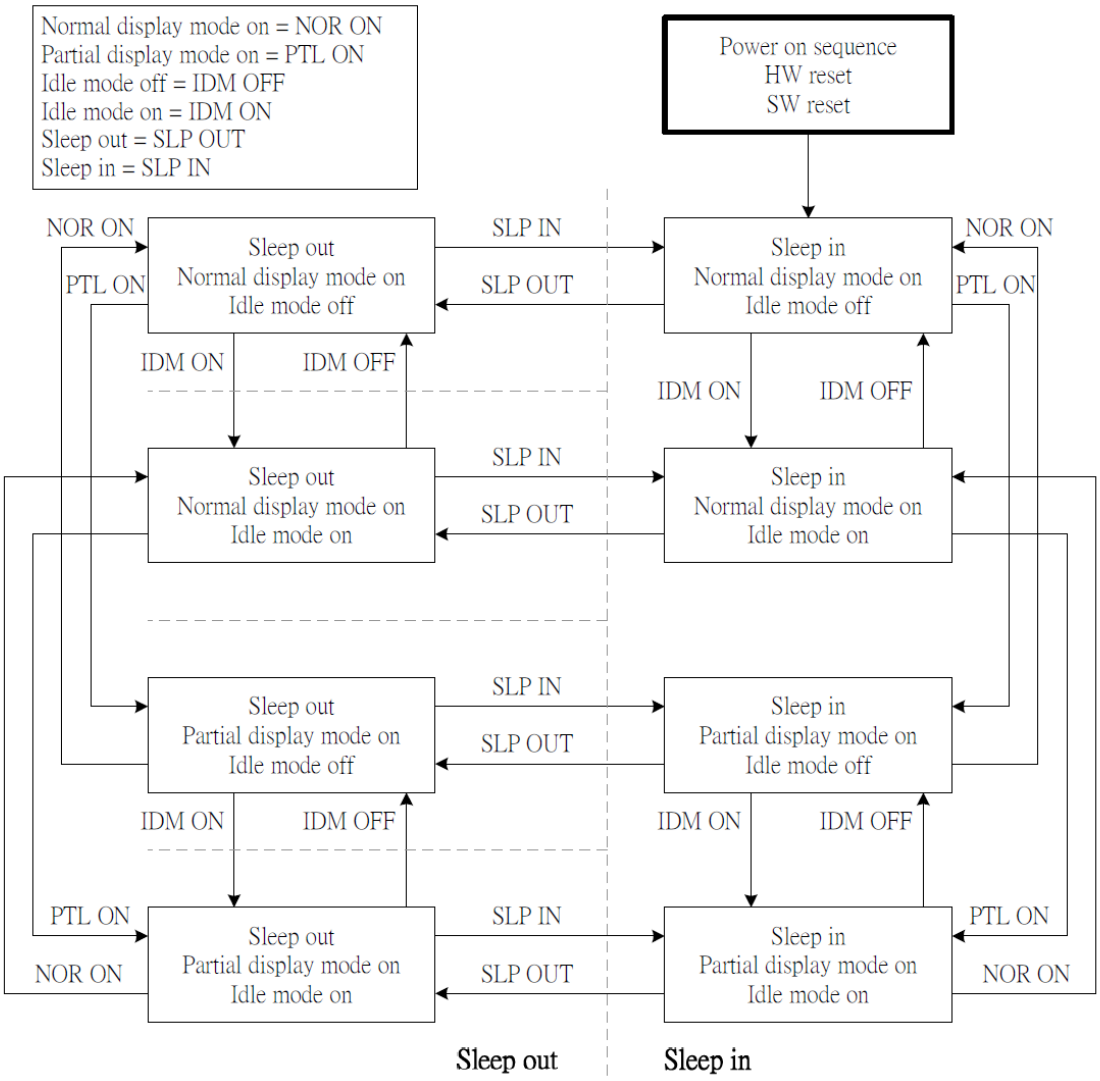
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode
   In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

7.3 Power Flow Chart

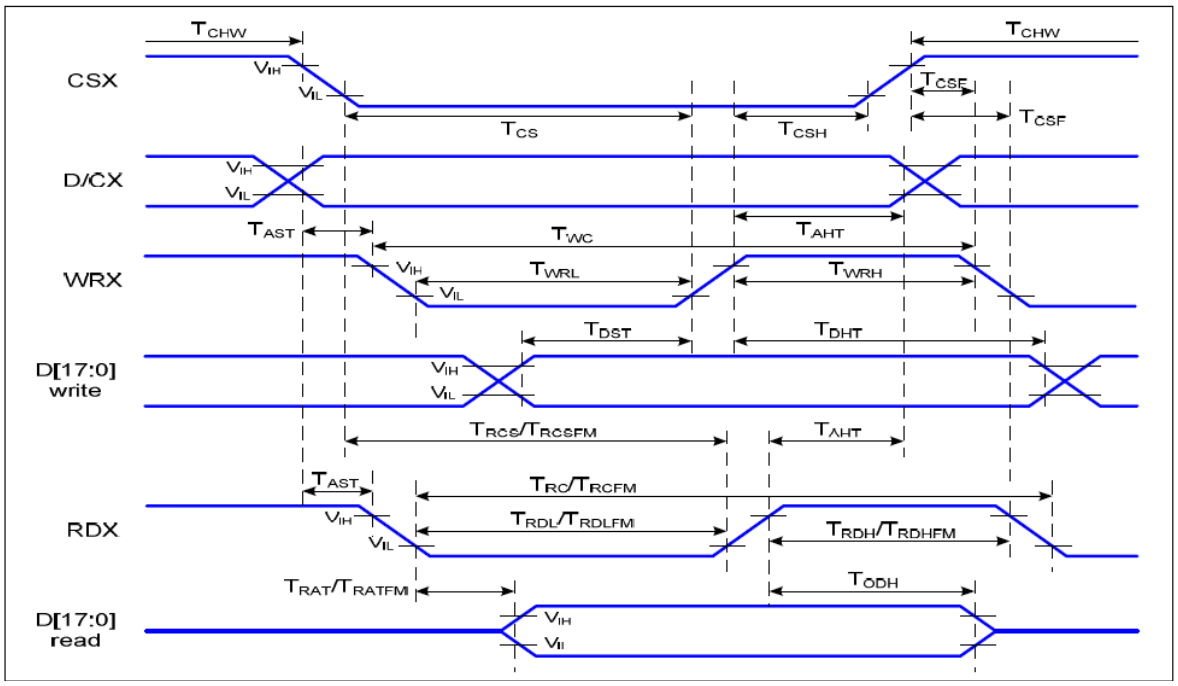


8 Electrical Characteristics

8.1 AC Characteristics (8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	



Parallel Interface Timing Characteristics (8080-Series MCU Interface)

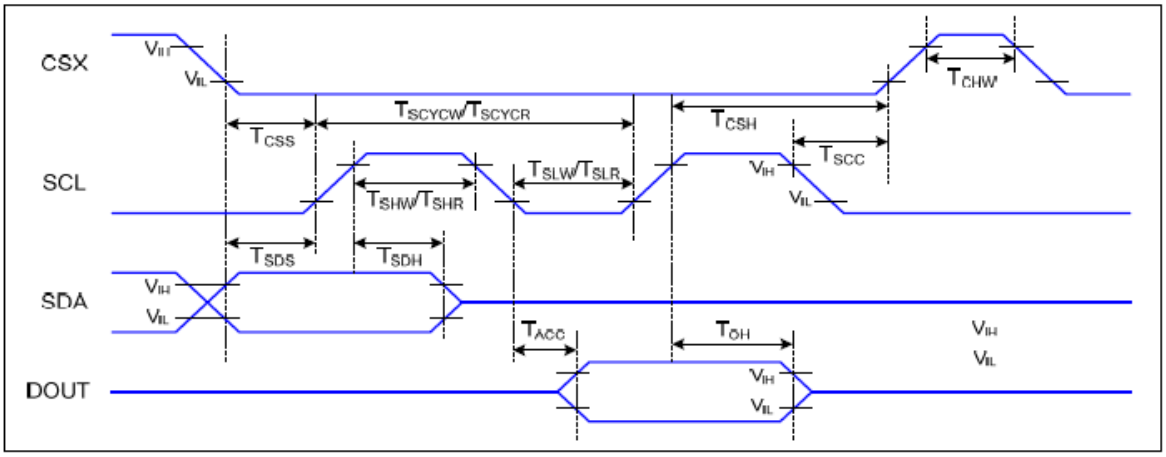
8.2 AC Characteristics (SPI Interface Timing Characteristics)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.


CSX
SCL
SDA
DOUT
VIH
VIL
TCSS
TSCYCW/TSCYCR
TCSH
TCHW
TSCC
TSHW/TSHR
TSLW/TSLR
TSDS
TSDH
TACC
TOH

8.3 3-Line Serial Interface

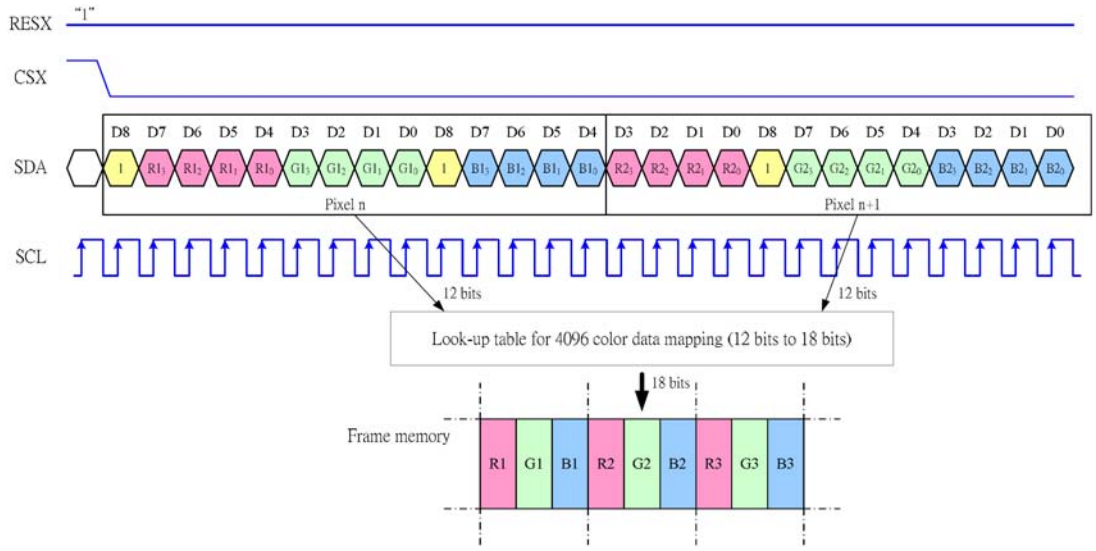
Different display data formats are available for three colors depth supported by the LCM listed below.

4k colors, RGB 4-4-4-bit input

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

Write data for 12-bit/pixel (RGB-4-4-4 bit input), 4K-Colors, 3Ah="03h"

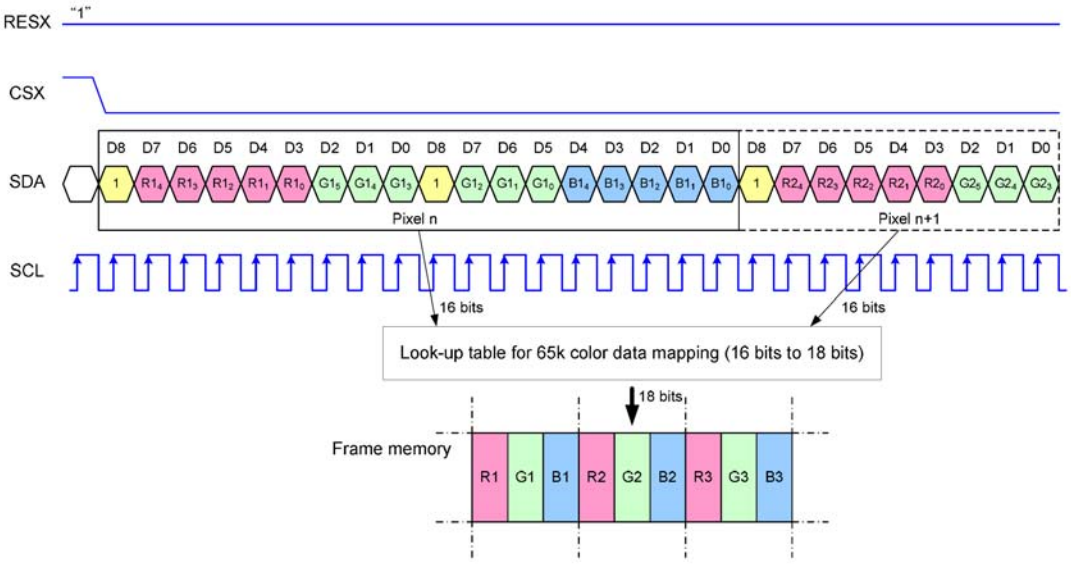


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"

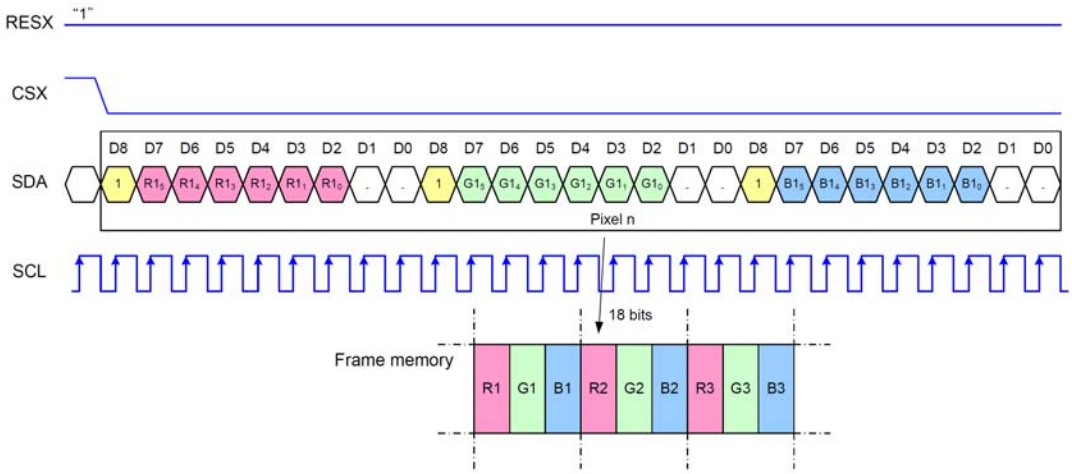


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah=”06h”



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.4 RGB Interface

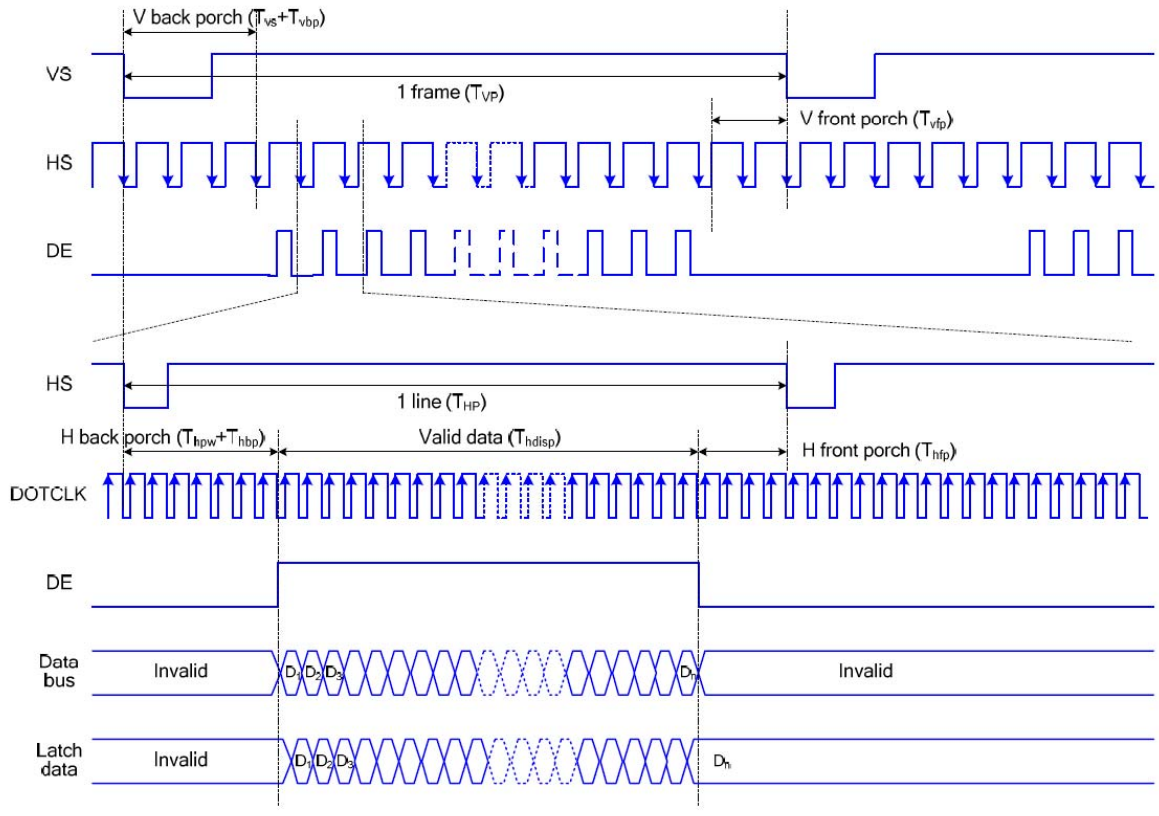
8.4.1 RGB Interface Mode Selection

ST7789V supports two kinds of RGB interface, DE mode and HV mode. Each mode also can select with ram and without ram. The table shown below uses command B1h to select RGB interface mode.

RCM[1:0]	WO	RGB Mode	Data Path
10	0	DE mode	Ram
	1		Shift register (without Ram)
11	0	HV mode	Ram
	1		Shift register (without Ram)

8.4.1 RGB Interface Timing

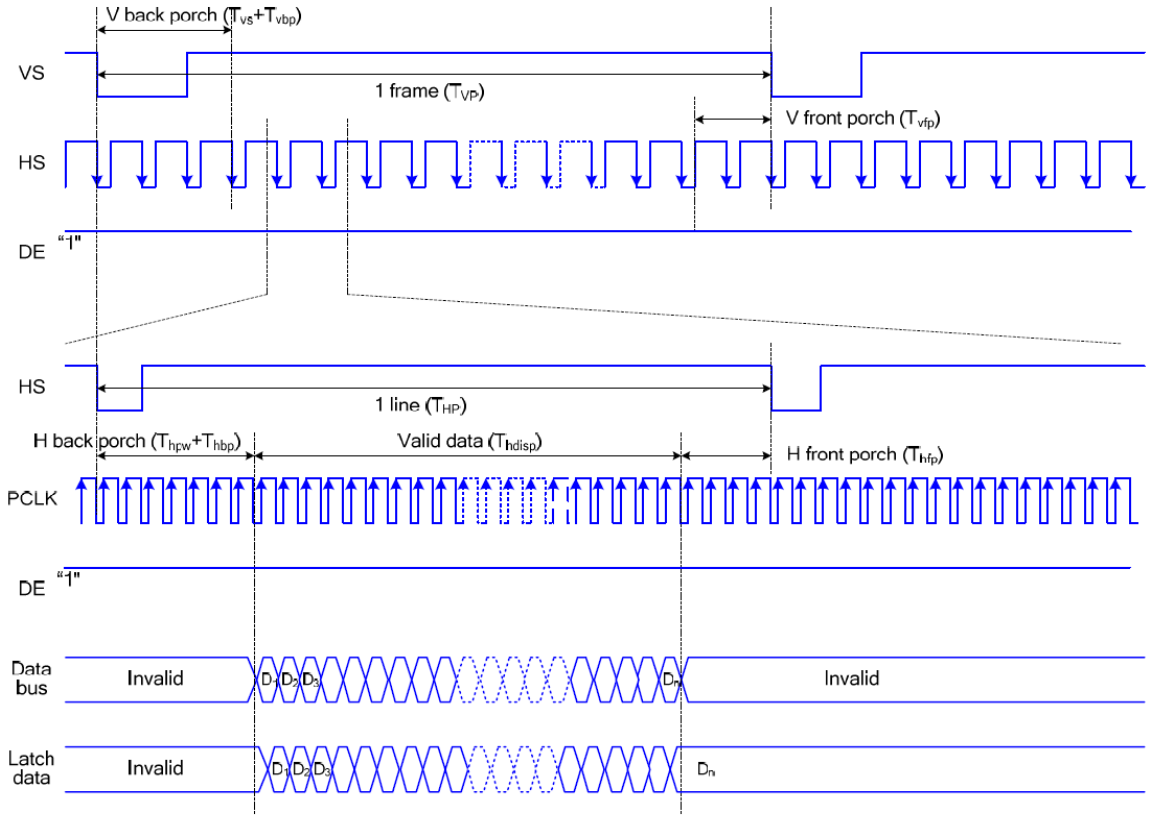
The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.



Timing chart of RGB interface HV mod

9 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=240 hrs	
Low Temperature Operation	-20±3°C , t=240 hrs	
High Temperature Storage	80±3°C , t=240 hrs	1,2
Low Temperature Storage	-30±3°C , t=240 hrs	1,2
Storage at High Temperature and Humidity	60°C, 90% RH , 240 hrs	1,2
Thermal Shock Test	-20°C (30min) ~ 70°C (30min) 100 cycles	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

10 USE PRECAUTIONS

10.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

10.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

10.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

10.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.

7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

10.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver.
3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

11 MECHANIC DRAWING