晶采光電科技股份有限公司
AMPIRE CO., LTD

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	**AM-240320D5TOQW-00H(R)**
APPROVED BY	
DATE	

☑ Approved For Specifications
☐Approved For Specifications & Sample

AMPIRE CO., LTD.
2F., No.88, Sec. 1, Sintai 5th Rd., Sijhih City, Taipei County 221, Taiwan (R.O.C.)台北縣汐止市新台五路一段88號2樓(東方科學園區D棟)
TEL:886-2-26967269 , FAX:886-2-86967196 or 26967270

APPROVED BY	CHECKED BY	ORGANIZED BY

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2010/07/01	-	New Release	Emil

1 Features

LCD 3.2 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) for mobile-phone or handy electrical equipments.

(1) Construction: 3.2" a-Si color TFT-LCD, White LED Backlight and FPCB.

(2) Main LCD : 2.1 Amorphous-TFT 3.2 inch display, transmissive, Normally white type, 9 o'clock.
2.2 240(RGB)X320 dots Matrix,1/320 Duty.
2.3 Narrow-contact ledge technique.
2.4 Main LCD Driver IC: RM68050 equivalent.
2.5 262K: Red-6bit, Green-6bit, Blue-6bit (18-bit interface)

(3) Low cross talk by frame rate modulation

(4) Direct data display with display RAM

(5) Partial display function: You can save power by limiting the display space.

(6) Interface: MPU and RGB Interface. (Select by H/W Jumper). Default: MCU Interface.

(7) SPI and Digital RGB 18-bit interface selectable.

IM3	**IM2**	**IM1**	**IM0**	**MPU mode**	**DB Pin in use**	**Remark**
PIN9	**JP2**	**PIN8**	**PIN7**			
0	0 (2,3Short)	1	0	80-16BIT	DB[17:10],DB[8:1]	MCU Interface.
0	0 (2,3Short)	1	1	80-8BIT	DB[17:10]	
1	0 (2,3Short)	1	0	80-18BIT	DB[17:0]	
1	0 (2,3Short)	1	1	80-9BIT	DB[17:9]]	
0	1 (1,2Short)	0	ID	SPI	SDI ,SDO	Must change JP2; SPI, RGB Interface

* Others setting invalid

(8) Abundant command functions:
Area scroll function
Display direction switching function
Power saving function

Electric volume control function: you are able to program the temperature compensation function.

2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
Active Display Size		3.2 inch diagonal(81.28mm)	mm
Main LCD	Outline Dimension	55.64 (H) x 77.3(V)	mm
	Pixel pitch	0.2025 (H) x 0.2025(V)	mm
	Active area	48.6 (H) x 64.8 (V)	mm
	Number of Pixels	240(H)x320(V) pixels	mm

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+3.3	V	
Power voltage	LED A – LED K	-0.5	+4.0	V	Parallel
Input voltage	VIN	-0.5	VDD	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +80°C Min. -30°C	Note 1: Non-condensing
Operating temperature	Max. +70°C Min. -10°C	Note 1: Non-condensing

Note 1：Ta≦+40°C・・・・Max.85%RH

Ta＞+40°C・・・・The max. humidity should not exceed the humidity with 40°C 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCM

(V_{DD}=3.0V, Ta=25 ^{o}C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{DD}		2.6	2.8	3.3	V
High-level input voltage	V_{IHC}		0.8		V_{DD}	V
Low-level input voltage	V_{ILC}		-0.3		0.2V_{DD}	V
Consumption current of VDD	I_{DD}	LED OFF	-	10	-	mA
Consumption current of LED	I_{LED_ON}	V_{LED}=19.2V	-	15	20	mA

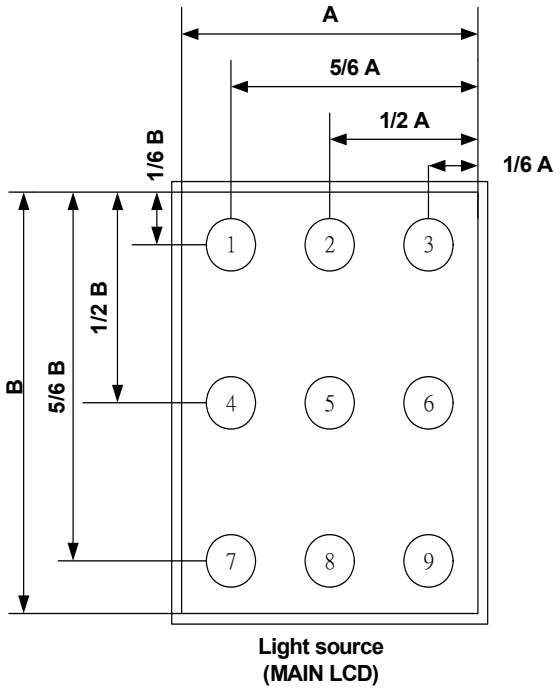
※ 1. 1/320 duty.

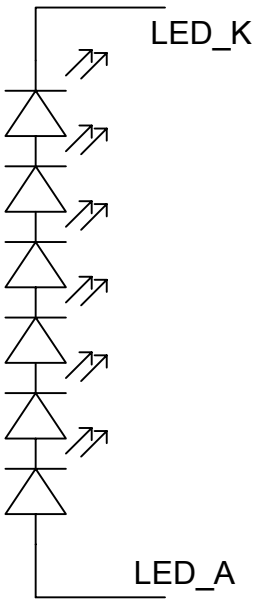
4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =15mA	-	(19)	-	V
Forward current	I_f	Vf=19V	-	(15)	(20)	mA
Uniformity (with L/G)	-	I_f=15mA	70%	-	-	
C.I.E.	X		0.265	0.30	0.335	
	Y		0.275	0.31	0.345	
Luminous color	White					
Chip connection	6 chip serial connection					

Note: (value), value=estimate value.

Bare LED measure position:





*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 80\%$

5 Main LCD

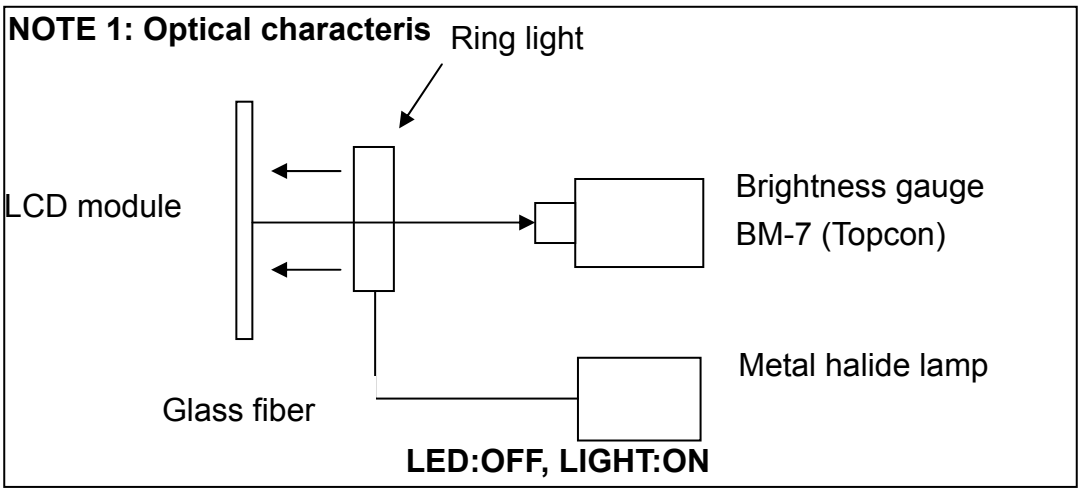
5-1 Optical characteristics

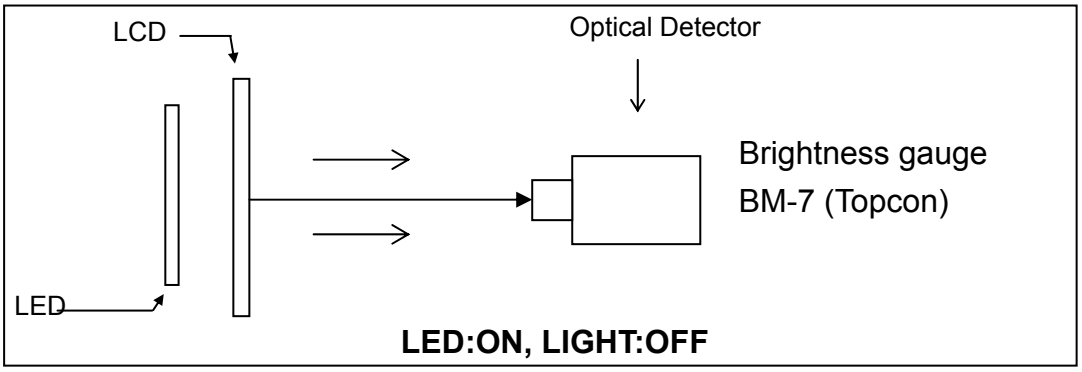
(1/320 Duty in case except as specified elsewhere Ta = 25°C)

Item		Symbol	Min.	Std.	Max.	Unit	Conditions
Contrast ratio		CR	150	200	-	-	θ=0° Φ=0° Normal viewing angle
Response time	Rising	Tr	-	15	-	ms	
	Faling	Tf	-	35	-		
White luminance (center of screen)		Y_L		200		cd/m2	
Color chromaticity (CIE1931)	Red	Rx	0.54	0.59	0.63		
		RY	0.30	0.34	0.38		
	Green	Gx	0.29	0.33	0.37		
		GY	0.56	0.60	0.64		
	Blue	Bx	0.10	0.14	0.18		
		BY	0.02	0.06	0.10		
	White	Wx	0.26	0.30	0.34		
		WY	0.27	0.31	0.35		
Visual angle	Hor.	θ_L	(38.7)			Degree	CR>10
		θ_R	(15)				
	Ver.	Θ_f	(62.7)				
		θ_b	(62.2)				

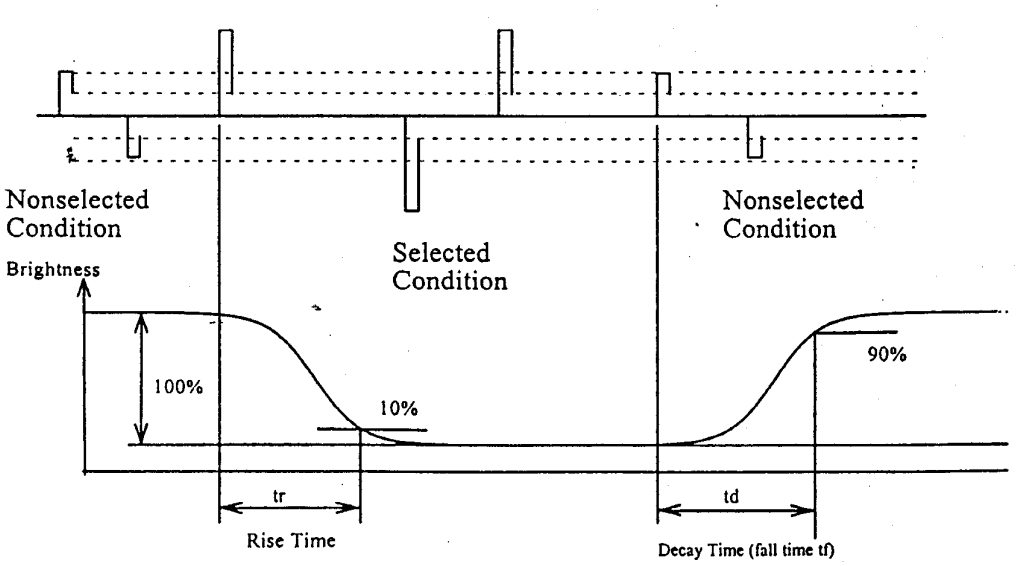
Note: (value), value=estimate value.

NOTE 1: Optical characteris

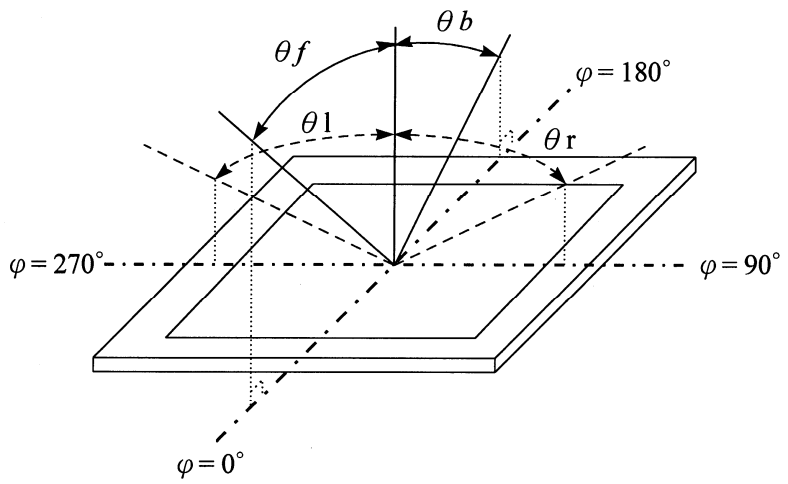




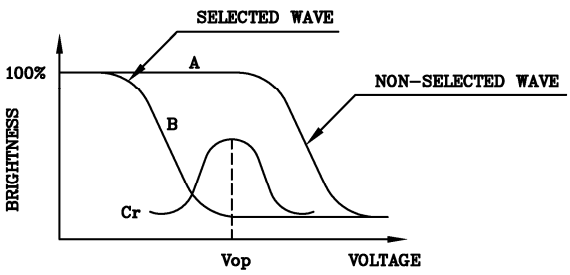
NOTE 2: Response tome definition



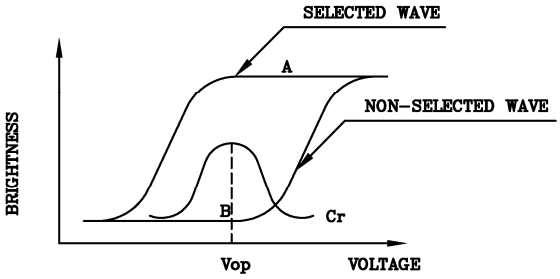
NOTE 3: φ、θ definition



NOTE 4: Contrast definition



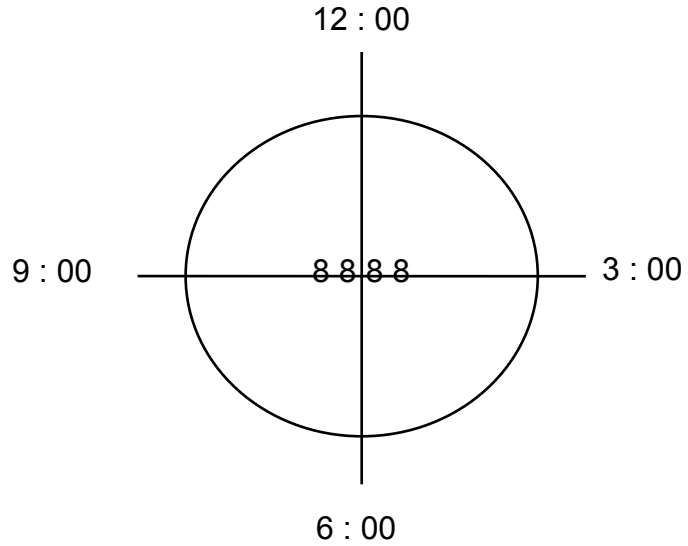
(positive type)



(negative type)

Contrast Ratio : Cr=A/B

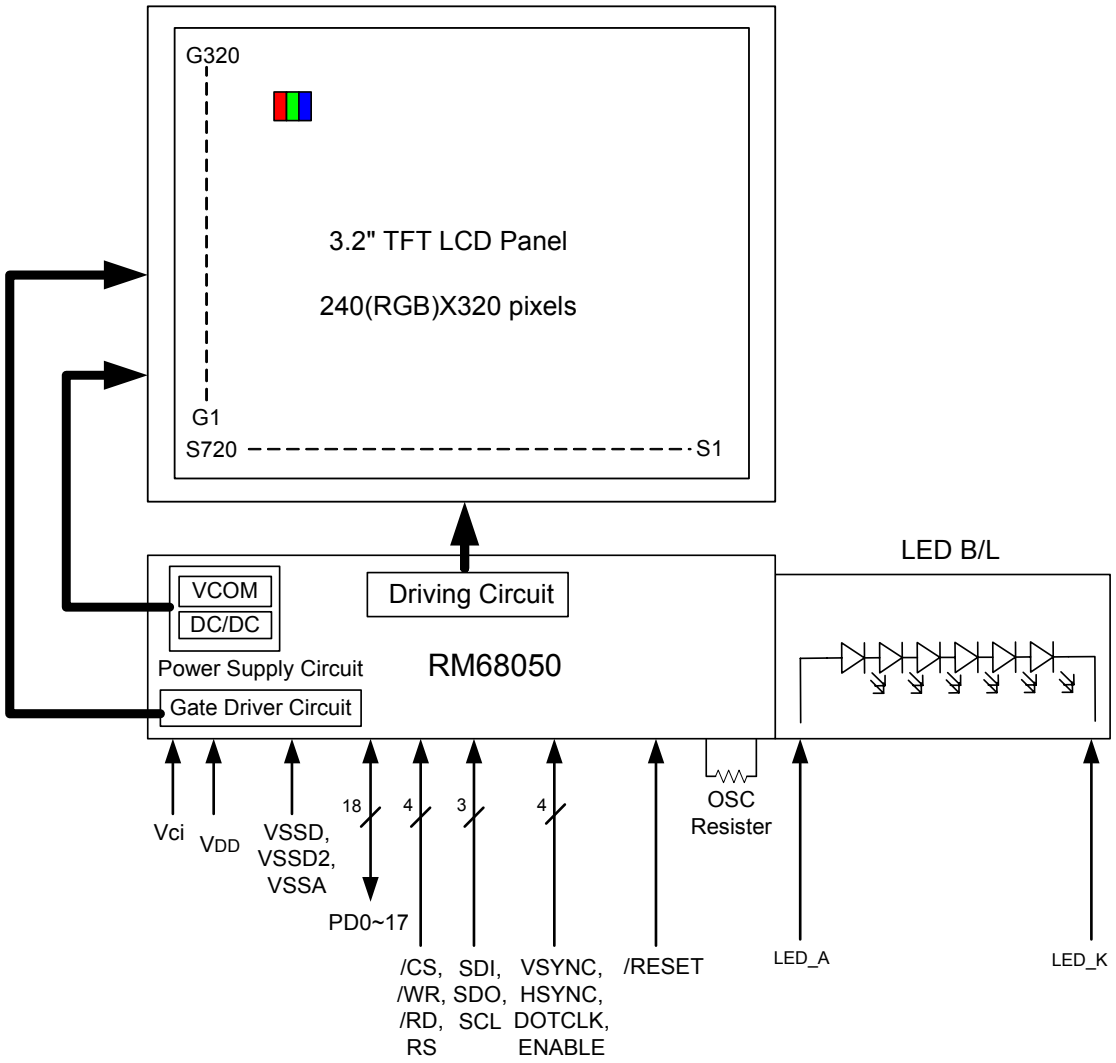
NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format: A-Si TFT transmissive, normally white type, 9 o'clock.
Display composition: 240 x RGB x 320 dots
LCD Driver: RM68050 or equivalent.



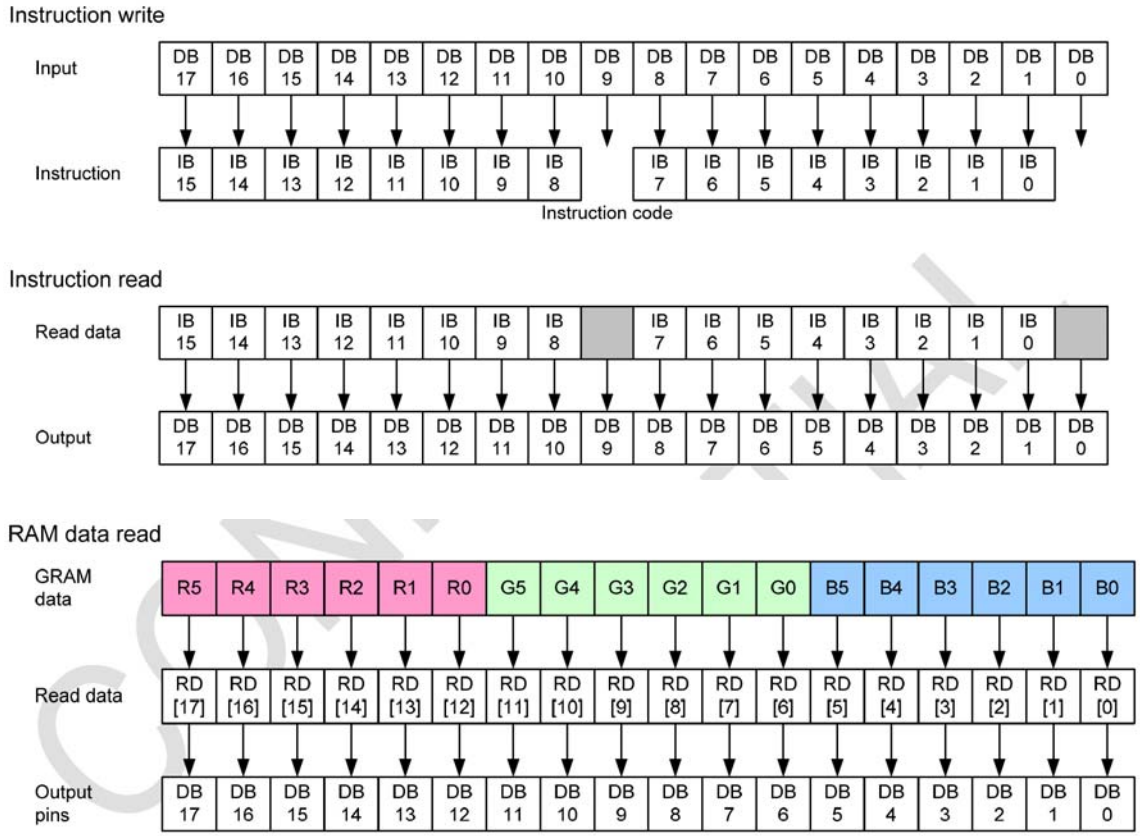
7 Interface specifications

Connecter pitch:0.3mm

Recommend Connecter: JAE FF0245S

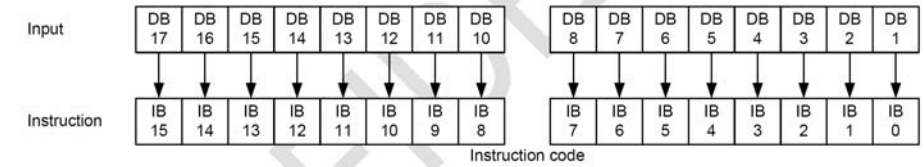
<table>
<tr><th>Pin No.</th><th>Terminal</th><th>Functions</th></tr>
<tr><td>1</td><td>VSS</td><td>Ground pins.</td></tr>
<tr><td>2</td><td>XL</td><td>Touch Panel Left Side.</td></tr>
<tr><td>3</td><td>XR</td><td>Touch Panel Right Side.</td></tr>
<tr><td>4</td><td>YD</td><td>Touch Panel Down Side.</td></tr>
<tr><td>5</td><td>YU</td><td>Touch Panel Up Side.</td></tr>
<tr><td>6</td><td>VSS</td><td>Ground pins.</td></tr>
<tr><td>7</td><td>IM0/ID</td><td rowspan="6"><table>
<tr><th>IM3</th><th>IM1</th><th>IM0/ID</th><th>MPU-Interface Mode</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>i80-system 16-bit interface</td><td>DB[17:10], DB[8:1]; (JP1 2-3short)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>i80-system 8-bit interface</td><td>DB[17:10]; (JP1 2-3short)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>i80-system 18-bit interface</td><td>DB[17:0]; (JP1 2-3short)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>i80-system 9-bit interface</td><td>DB[17:9]; (JP1 2-3short)</td></tr>
<tr><td>0</td><td>0</td><td>ID</td><td>Serial Peripheral Interface</td><td>SDI, SDO; (JP1 1-2short)</td></tr>
</table></td></tr>
<tr><td>8</td><td>IM1</td></tr>
<tr><td>9</td><td>IM3</td></tr>
<tr><td>10</td><td>SDO</td><td>Serial bus interface data output pin.</td></tr>
<tr><td>11</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>12</td><td>SDI</td><td>Serial bus interface data input pin.</td></tr>
<tr><td>13-30</td><td>D17-D0</td><td>18-bit bidirectional bus
Connect to VSS when the serial interface is selected.</td></tr>
<tr><td>31</td><td>/CS</td><td>Chip selection pin.
The “L” level enables inputting commands and reading /writing data.</td></tr>
<tr><td>32</td><td>/RESET</td><td>Switching to “L” initializes internally.
Must be reset after the power is supplied.</td></tr>
<tr><td>33</td><td>RS</td><td>Command/display Data Selection.</td></tr>
<tr><td>34</td><td>WR/SCL</td><td>Write enable signal/Serial bus interface clock input pin.</td></tr>
<tr><td>35</td><td>/RD</td><td>Read enable signal.</td></tr>
<tr><td>36</td><td>VSYNC</td><td>Frame synchronizing signal in RGB I/F mode. (JP1 1-2short)</td></tr>
<tr><td>37</td><td>HSYNC</td><td>Frame synchronizing signal in RGB I/F mode. (JP1 1-2short)</td></tr>
<tr><td>38</td><td>DOTCLK</td><td>Dot clock signal in RGB I/F mode. (JP1 1-2short)</td></tr>
<tr><td>39</td><td>ENABLE</td><td>A data ENABLE signal in RGB I/F mode. (JP1 1-2short)</td></tr>
<tr><td>40</td><td>VCC</td><td rowspan="2">Power supply for Step-up circuit. (VCI=2.5~3.3V).</td></tr>
<tr><td>41</td><td>VCC</td></tr>
<tr><td>42</td><td>VSS</td><td>Ground pins.</td></tr>
<tr><td>43</td><td>LED_K</td><td>Power supply for LED (Cathode).</td></tr>
<tr><td>44</td><td>LED_A</td><td>Power supply for LED (Anode).</td></tr>
<tr><td>45</td><td>VSS</td><td>Ground pins.</td></tr>
</table>

7-1 80-system 18-bit interface

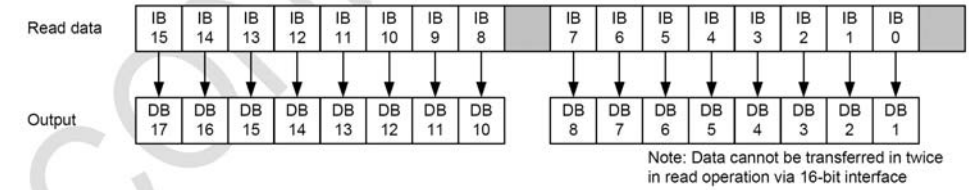


7-2 80-system 16-bit interface

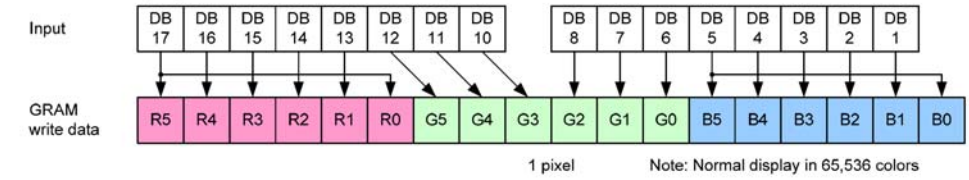
Instruction write



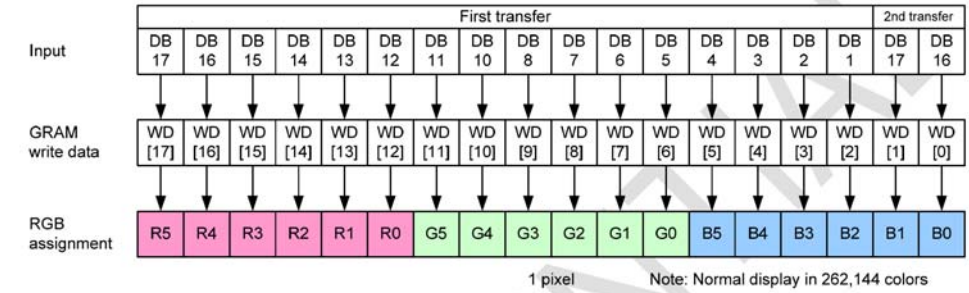
Instruction read



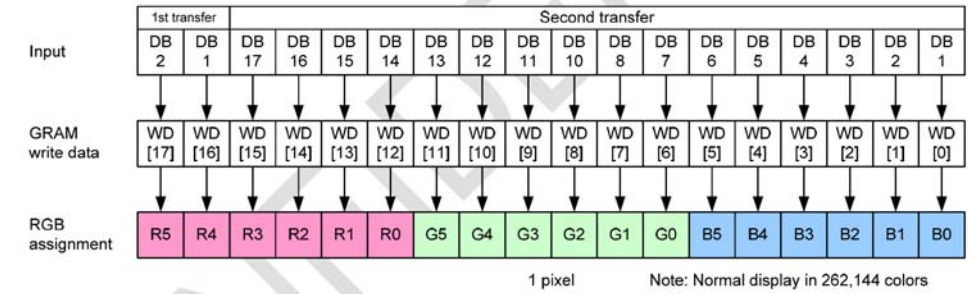
RAM data write (single transfer mode: TRIREG = 0)



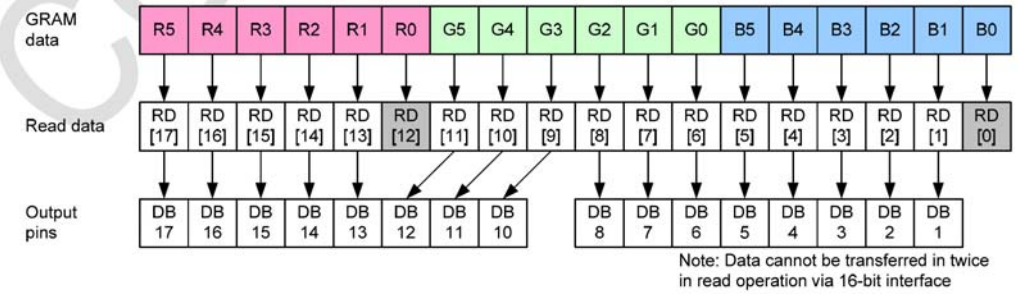
RAM data write (2 transfer mode: TRIREG = 1, DFM = 0)



RAM data write (2 transfer mode: TRIREG = 1, DFM = 1)

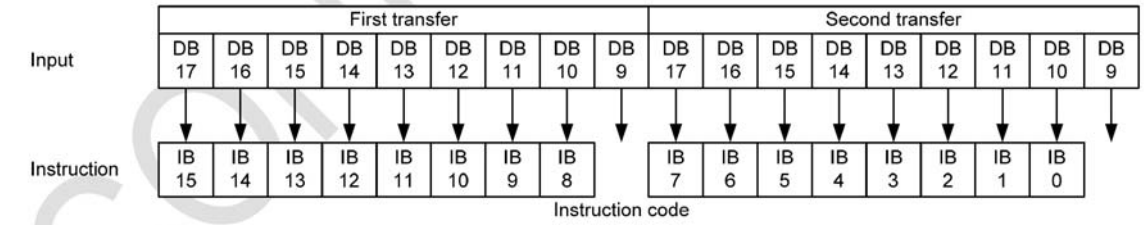


RAM data read (single transfer: TRIREG = 0)

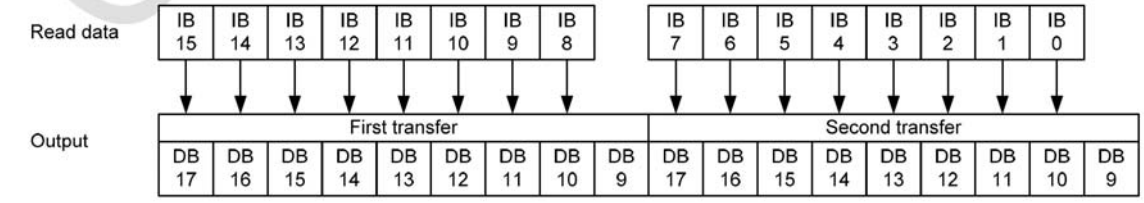


7-3 80-system 9-bit interface

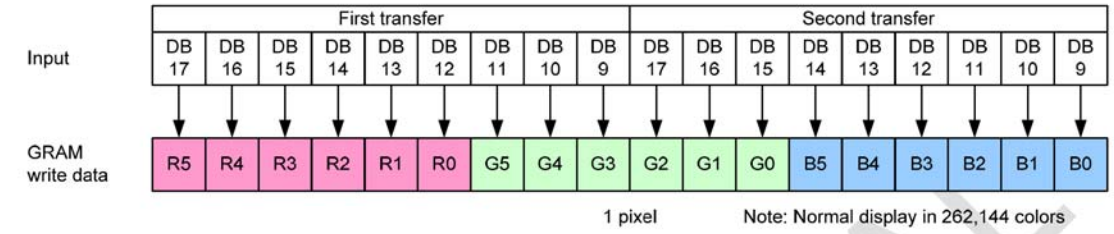
Instruction write



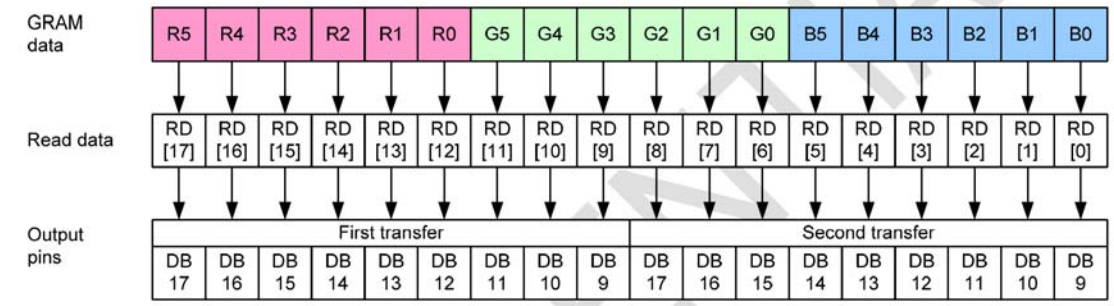
Device code read



RAM data write

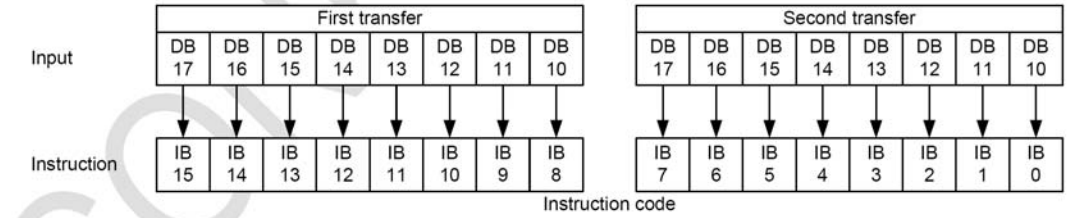


RAM data read

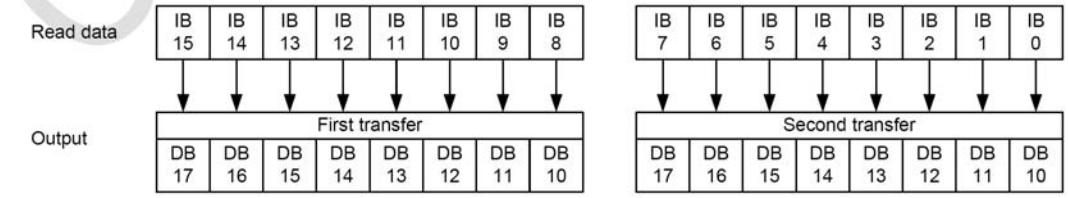


7-4 80-system 8-bit interface

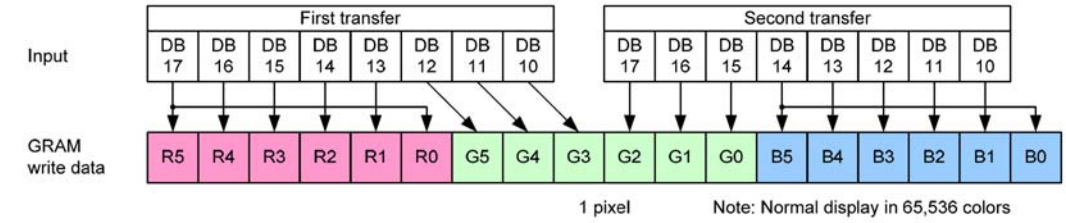
Instruction write



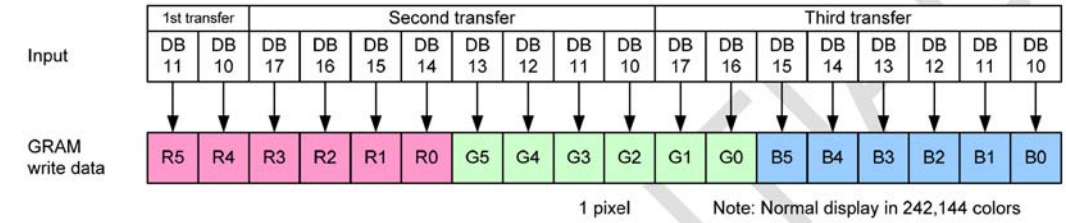
Device code read



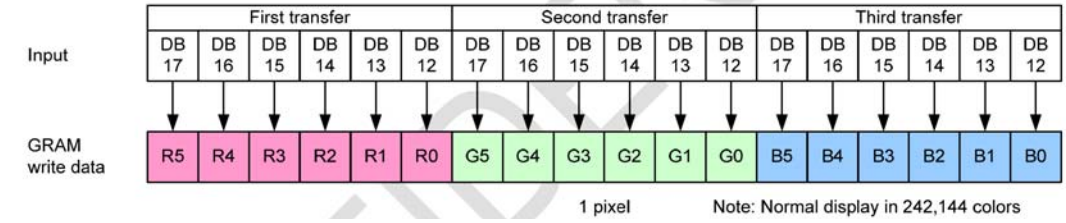
RAM data write (2-transfer mode: TRIREG = 0)



RAM data write (3-transfer mode: TRIREG = 1, DFM = 0)



RAM data write (3-transfer mode: TRIREG = 1, DFM = 1)



7-5 Serial Peripheral interface (SPI)

The system interface of RM68050 also includes the Serial Peripheral Interface (SPI). In SPI mode (JP2 1, 2 short on FPC), /CS, SCL, SDI and SDO are used to transfer data between MCU and RM68050. IM0/ID pin served as the ID pin. Figure 7-9 illustrates the detail timing while using SPI. Be aware that the unused pins such as DB17-0 pins must be fixed at either IOVCC or GND level.

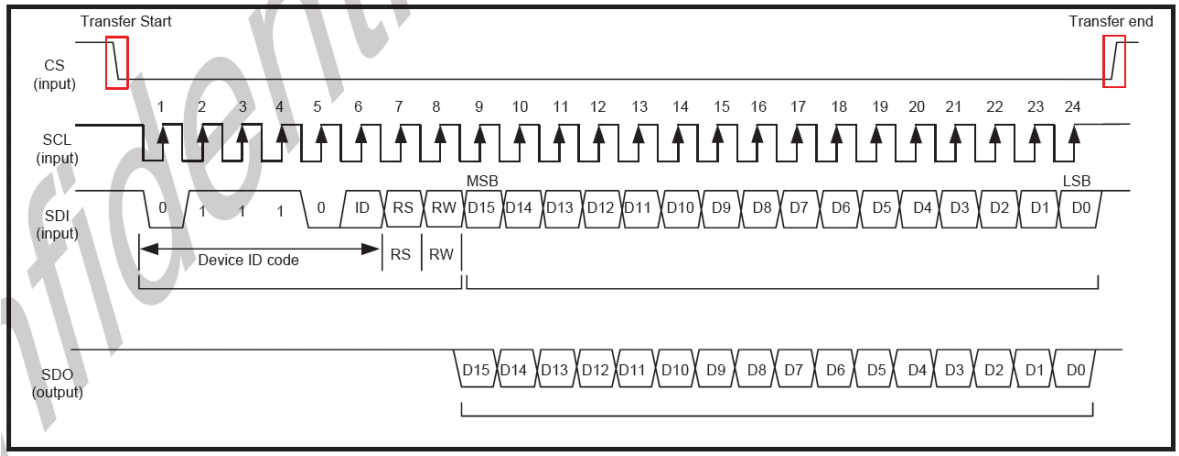


Figure 7-9

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

The instruction and GRAM accessing format o Serial Peripheral interface are shown in Figure 7-10 and Figure 7-11 respectively.

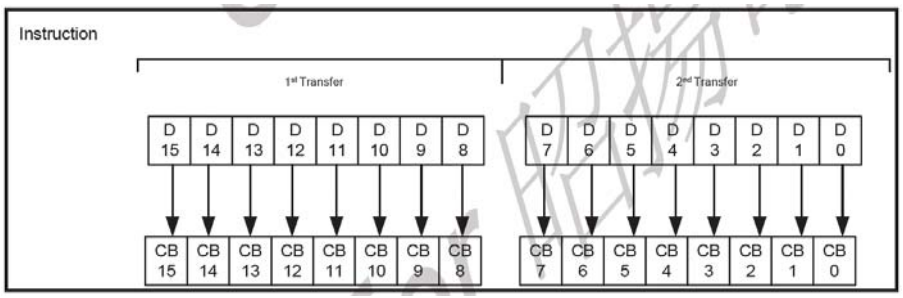


Figure 7-10

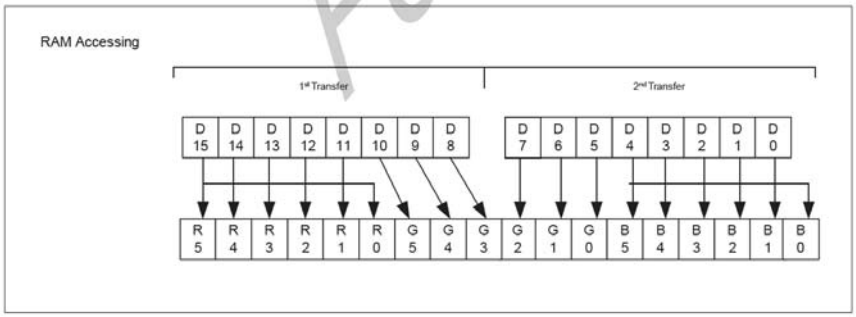


Figure 7-11

When read operation is desired In SPI mode, valid data are read out as the RM68050 reads out the 6th byte data from the internal GRAM. The RAM data transfer in SPI mode, in SPI mode with status read are illustrated in Figure 7-12,, respectively.

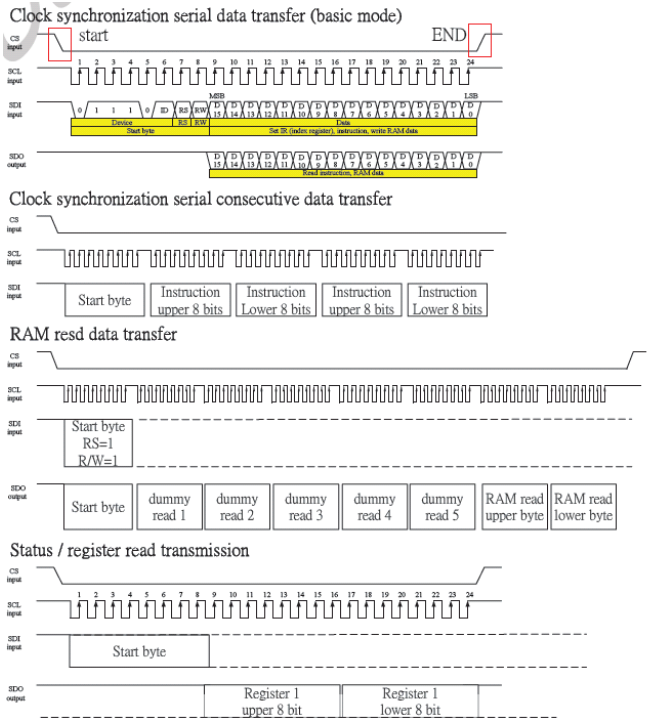


Figure 7-12

7-6 RGB Interface

AM-240320D5TOQW-00H also includes external (RGB) interface for displaying moving picture. External interface can be set by RIM1-0 bit. Table 7-1summarized the corresponding types of RGB interface with RIM1-0 setting.

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-10, 8-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting disabled	

Table 7-1

RGB interface cab access RM68050 by VSYNC, HSYNC, ENABLE, DOTCLK and DB17-0 signals, where VSYNC is used for frame synchronization; HSYNC is used for line synchronization and ENABLE is served as the valid data synchronized signals. The RGB interface can be rewriting minimum necessary data to the GRAM area which need to be overwritten with use of window address function and high-speed write mode. It is necessary for RGB interface to set front and back porch periods after and before a display period, respectively. Figure 7-13 illustrates the general timing for RGB interface. There are some constrain while using RGB interface. The following summarized the conditions

(a) Partial display/ scroll function / interlace and graphics operation function are not available for RGB interface.

(b) In RGB interface VSYNC, HSYNC, and DOTCLK signals must be input through a display operation period.

(c) The setting of the NO1-0 bits, STD1-0 bits and EQ1-0 bits are based on DOTCLK in RGB interface mode. In 6-bit RGB interface mode, it takes 3 DOTCLK inputs to transfer one pixel. Be aware data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode is necessary. Set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, DB17-0) to input 3x clock to complete data transfer in units of pixels.

(d) In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

(e) In RGB interface mode, a GRAM address (DB17-0) is set in the address counter every frame on the falling edge of VSYNC.

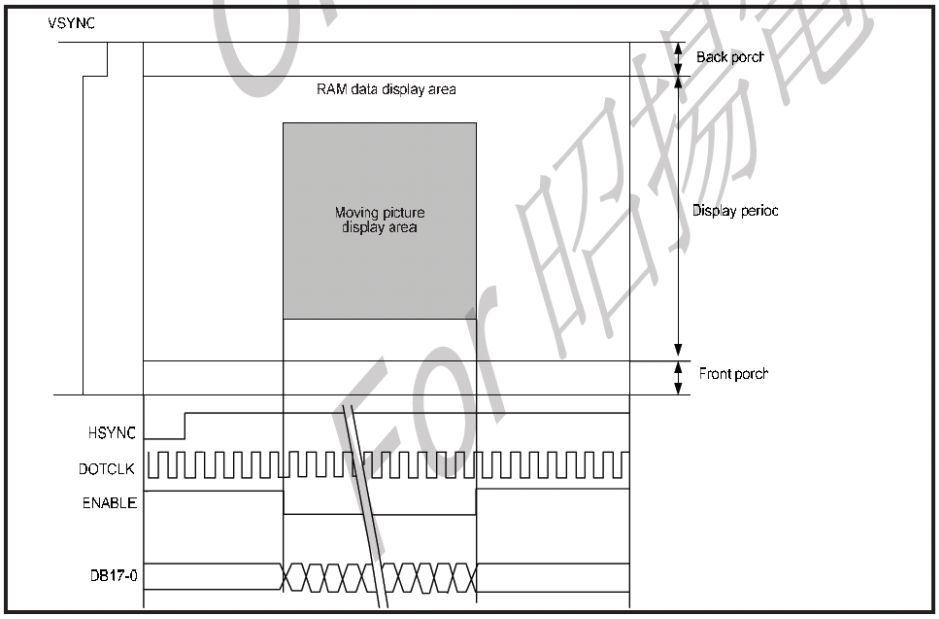


Figure 7-13

RGB interface includes ENABLE signal served as valid data synchronized signals. Moreover, the active level for ENABLE can be set by EPL. The EPL bit inverts the polarity of ENABLE signal. Table 7-2 summarized the setting of EPL and ENABLE active level for GRAM accessing. Setting both EPL and ENABLE bits to automatically update RAM address in the AC is necessary while writing data to the GRAM.

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disenabled	Retained
1	0	Disenabled	Retained
1	1	Enabled	Updated

Table 7-2

RM68050 can support 18-bit, 16-bit and 6-bit RGB interface. The detail timing diagram for 18-bit, 16-bit and 6-bit RGB interface are shown in Figure7-14 and Figure 7-15respectively.

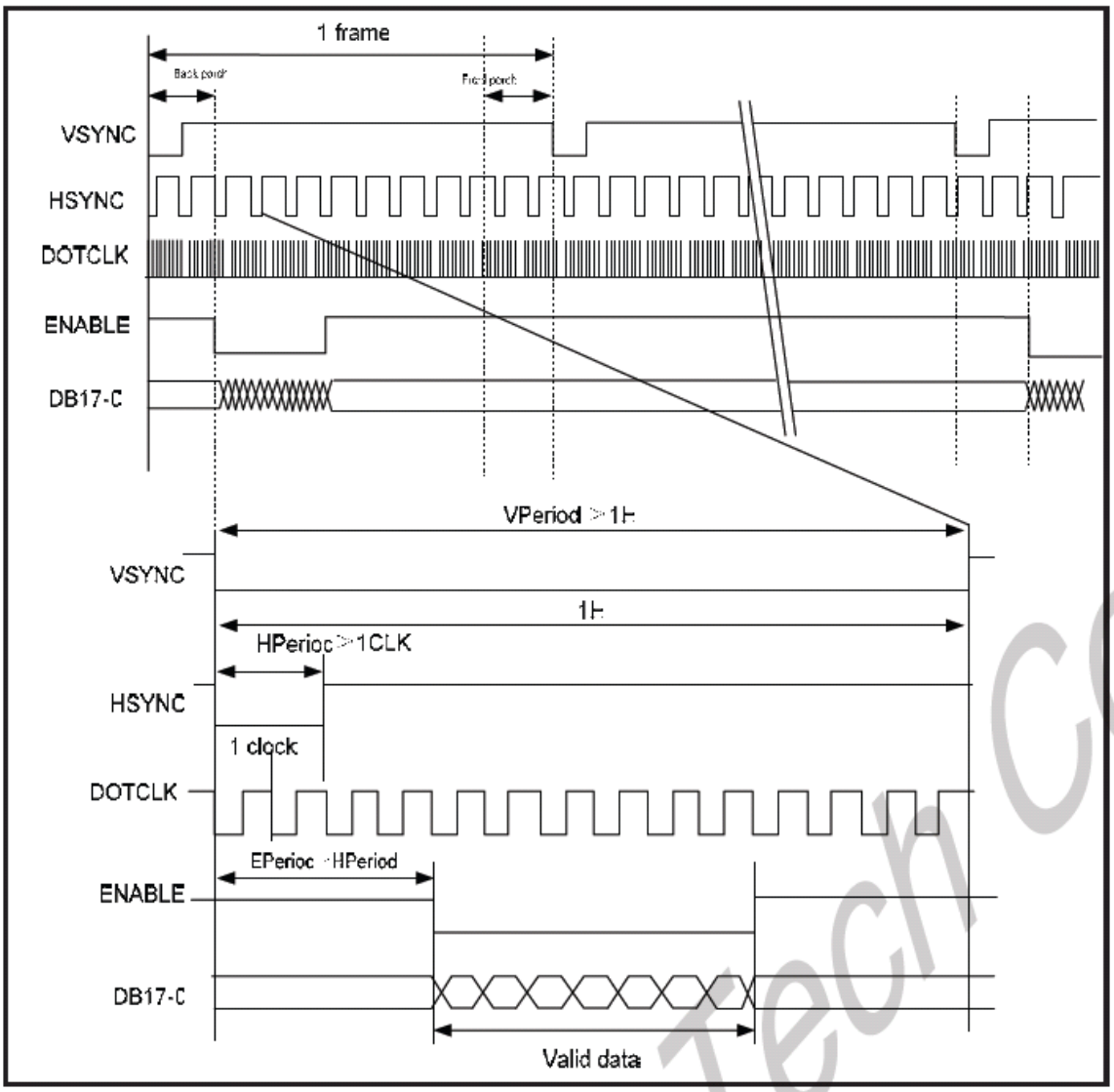


Figure 7-14

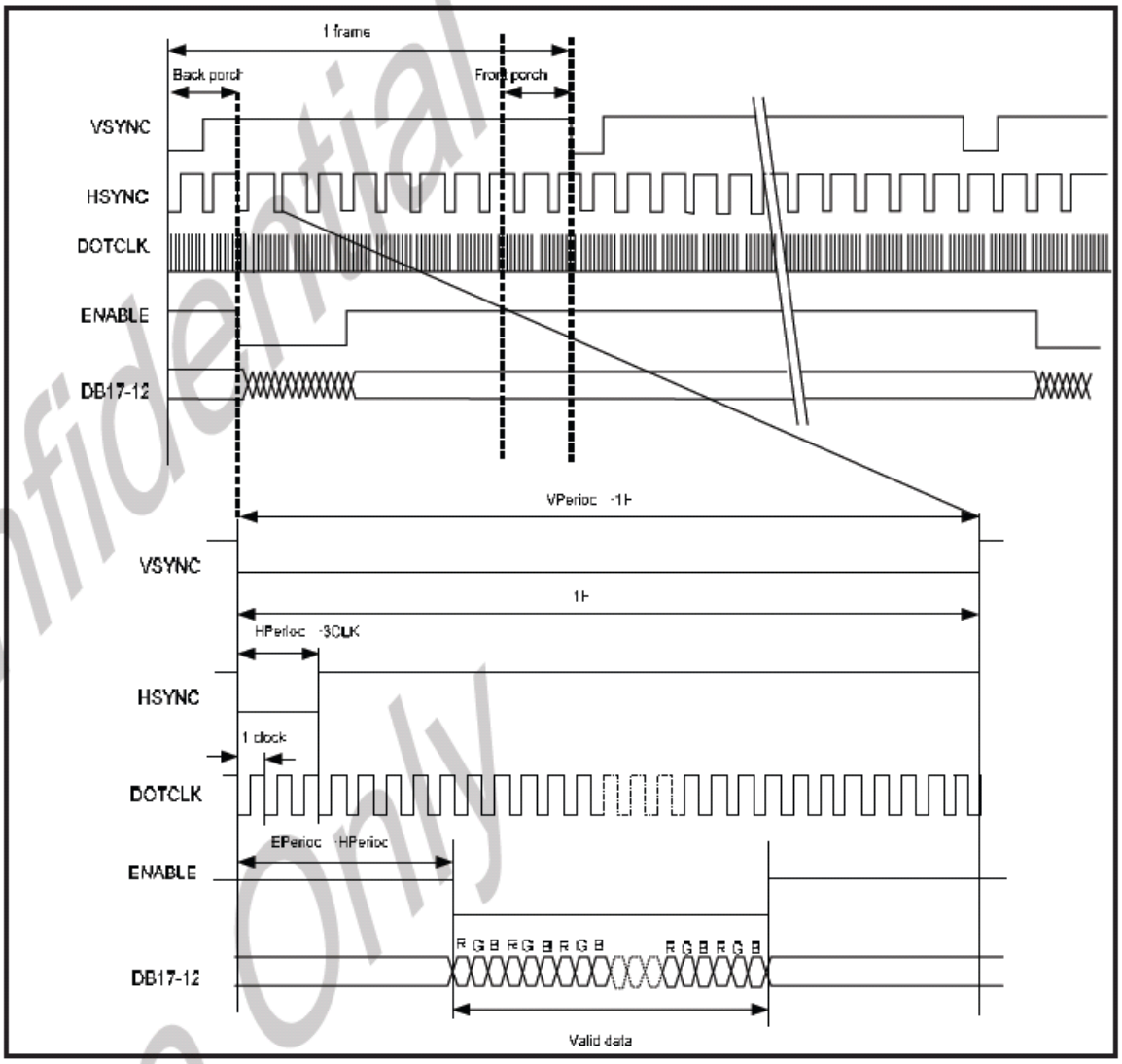

1 frame
Back porch
Front porch
VSYNC
HSYNC
DOTCLK
ENABLE
DB17-12
VPeriod -1H
VSYNC
1H
HPeriod -3CLK
HSYNC
1 clock
DOTCLK
EPeriod HPeriod
ENABLE
R G B R G B R G B
R G B R G B
DB17-12
Valid data

Figure 7-15

The RGB interface also has the window address function to transfer only minimum necessary data on the moving picture GRAM area, which can lower the power consumption and still can use system interface to rewrite data in still picture RAM area while displaying a moving picture. Setting RM = 0 while in RGB interface mode can make GRAM access through the system interface. When RGB interface accessing GRAM is desired, wait for one read/write bus cycle following by RM = 1 setting. Figure 7-16 illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

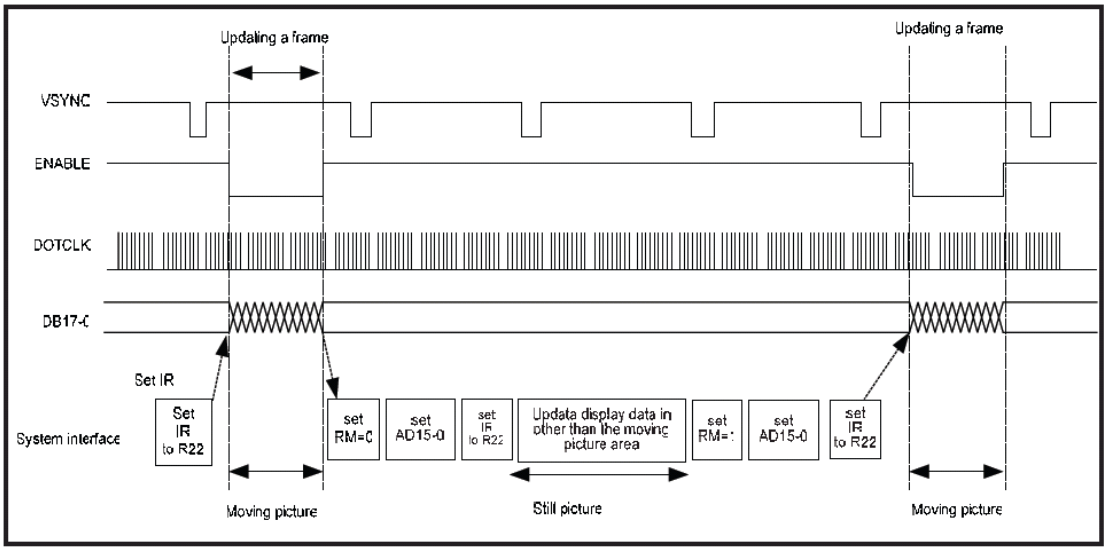


Figure 7-16

* 6-bit RGB interface

RAM accessing format and data transmission synchronization of 6-bit RGB interface are shown in Figure 7-17 and Figure 7-18, respectively.

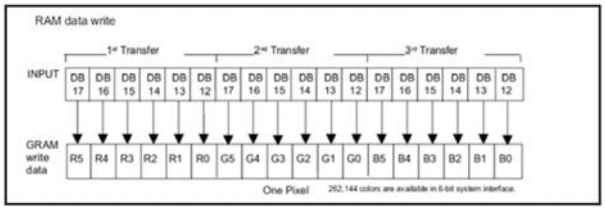


Figure 7-176

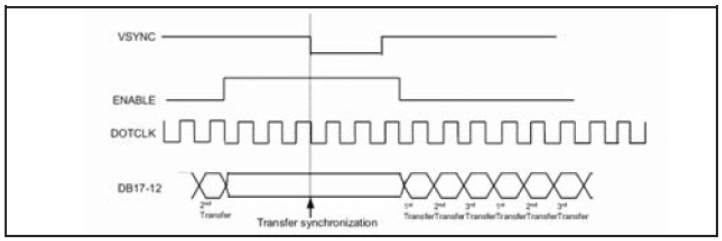


Figure 7-18

* 16-bit RGB interface

RAM accessing format of 16-bit RGB interface are shown in Figure 7-19.

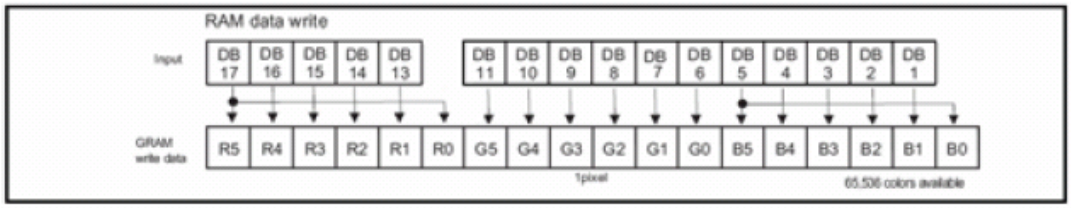


Figure 7-19

* 18-bit RGB interface

RAM accessing format of 18-bit RGB interface are shown in Figure 8-21.

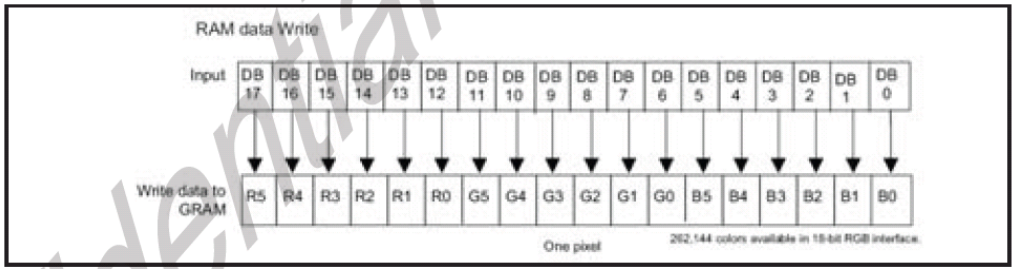


Figure 7-20

7-7 Instruction List

Main LCD Driver IC:RM68050

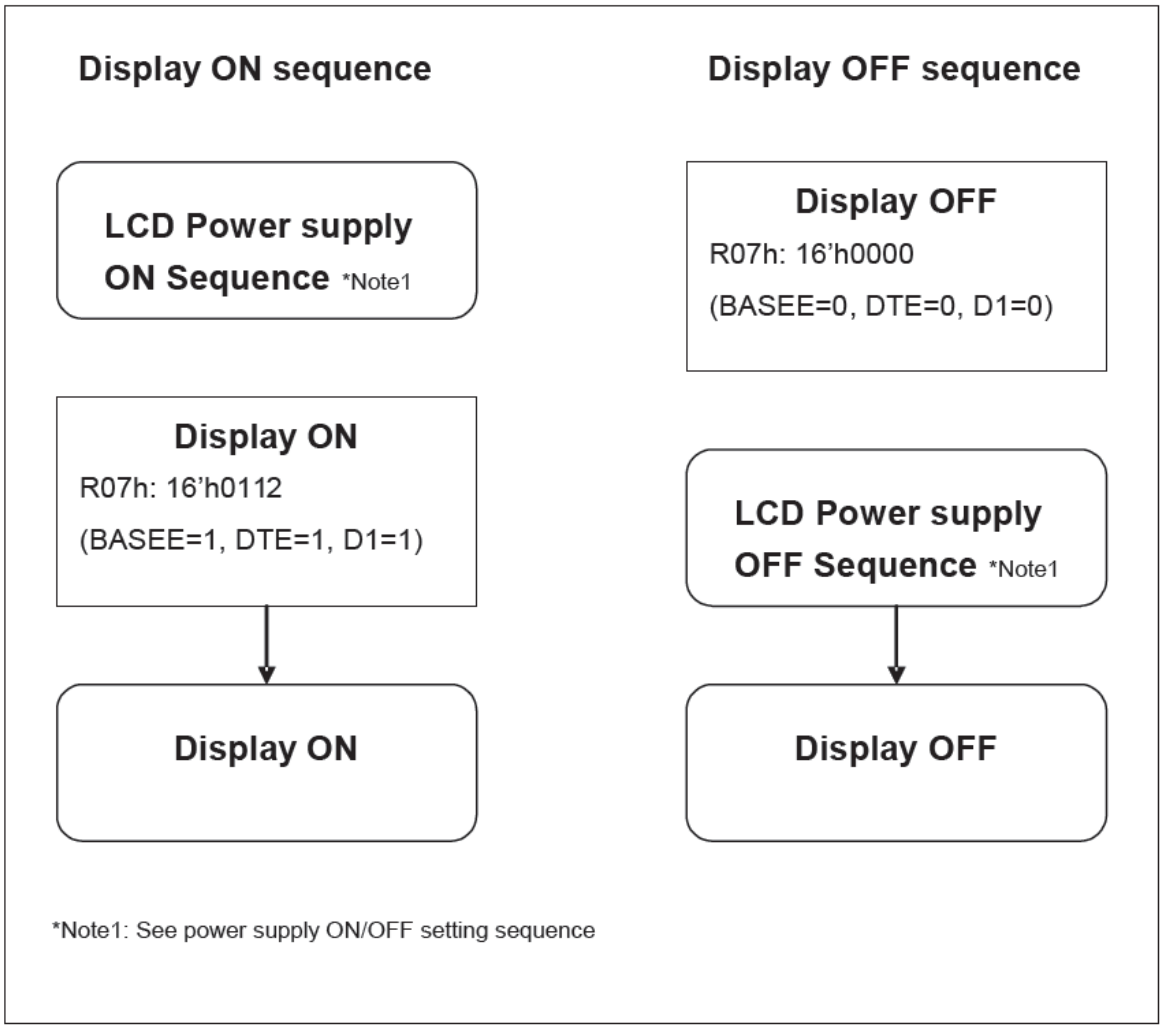
No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	RO	1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
05h	16 bits data format control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF1	EPF0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
10h	Power Control 1	W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS[3]	FRS[2]	FRS[1]	FRS[0]
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
66h	SPI Read/Write Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX (0)
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI00	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
A1h	OTP VCM Programming Control	W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_OTP5	VCM_OTP4	VCM_OTP3	VCM_OTP2	VCM_OTP1	VCM_OTP0
A2h	OTP VCM Status and Enable	W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
A5h	OTP Programming ID Key	W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
B1h	Write Display Brightness	W	1	X	X	X	X	X	X	X	X	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
B2h	Read Display Brightness	R	1	X	X	X	X	X	X	X	X	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
B3h	Write CTRL Display value	W	1	X	X	X	X	X	X	X	X	X	X	BCTRL	X	DD	BL	X	X
B4h	Read CTRL Display value	R	1	X	X	X	X	X	X	X	X	X	X	BCTRL	X	DD	BL	X	X
B5h	Write Content Adaptive Brightness Control value	W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	C[1:0]	

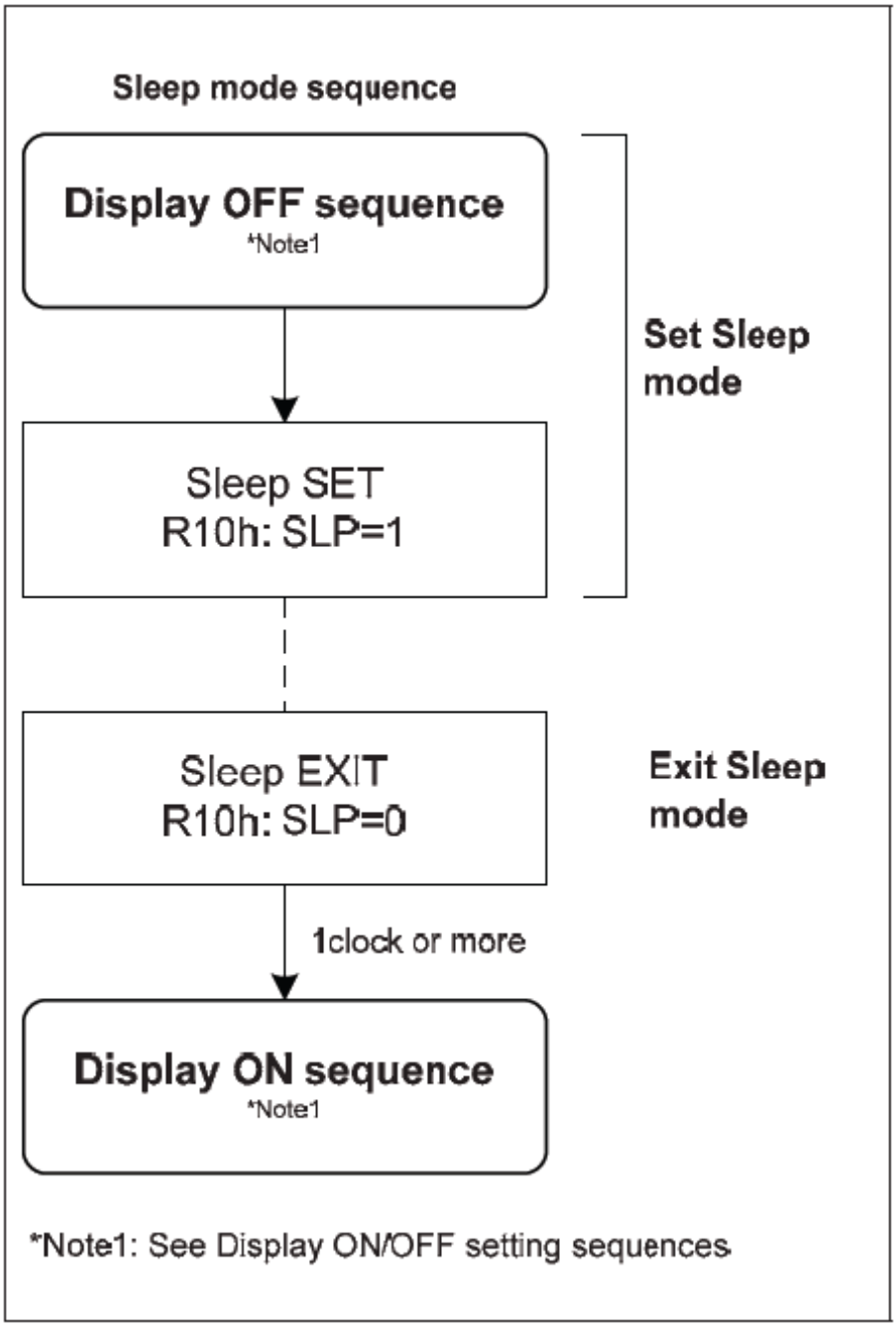
No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B6h	Read Content Adaptive Brightness Control value	R	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	C[1:0]	
BEh	Write CABC Minimum Brightness	W	1	X	X	X	X	X	X	X	X	CMB[7:0]							
BFh	Read CABC Minimum Brightness	R	1	X	X	X	X	X	X	X	X	CMB[7:0]							
C8h	CABC Control 1	W	1	X	X	X	X	X	X	X	X	PWM_DIV[7:0]							
C9h	CABC Control 2	W	1	X	X	X	X	X	X	X	X	THRES_MOV[3:0]				THRES_STILL[3:0]			
CAh	CABC Control 3	W	1	X	X	X	X	X	X	X	X	0	0	0	0	THRES_UI[3:0]			
CBh	CABC Control 4	W	1	X	X	X	X	X	X	X	X	DTH_MOV[3:0]				DTH_STILL[3:0]			
CCh	CABC Control 5	W	1	X	X	X	X	X	X	X	X	0	0	0	0	DTH_UI[3:0]			
CDh	CABC Control 6	W	1	X	X	X	X	X	X	X	X	DIM_OPT2[3:0]				0	DIM_OPT1[2:0]		
CEh	CABC Control 7	W	1	X	X	X	X	X	X	X	X	SCD_VLINE[8:0]							

8 Application

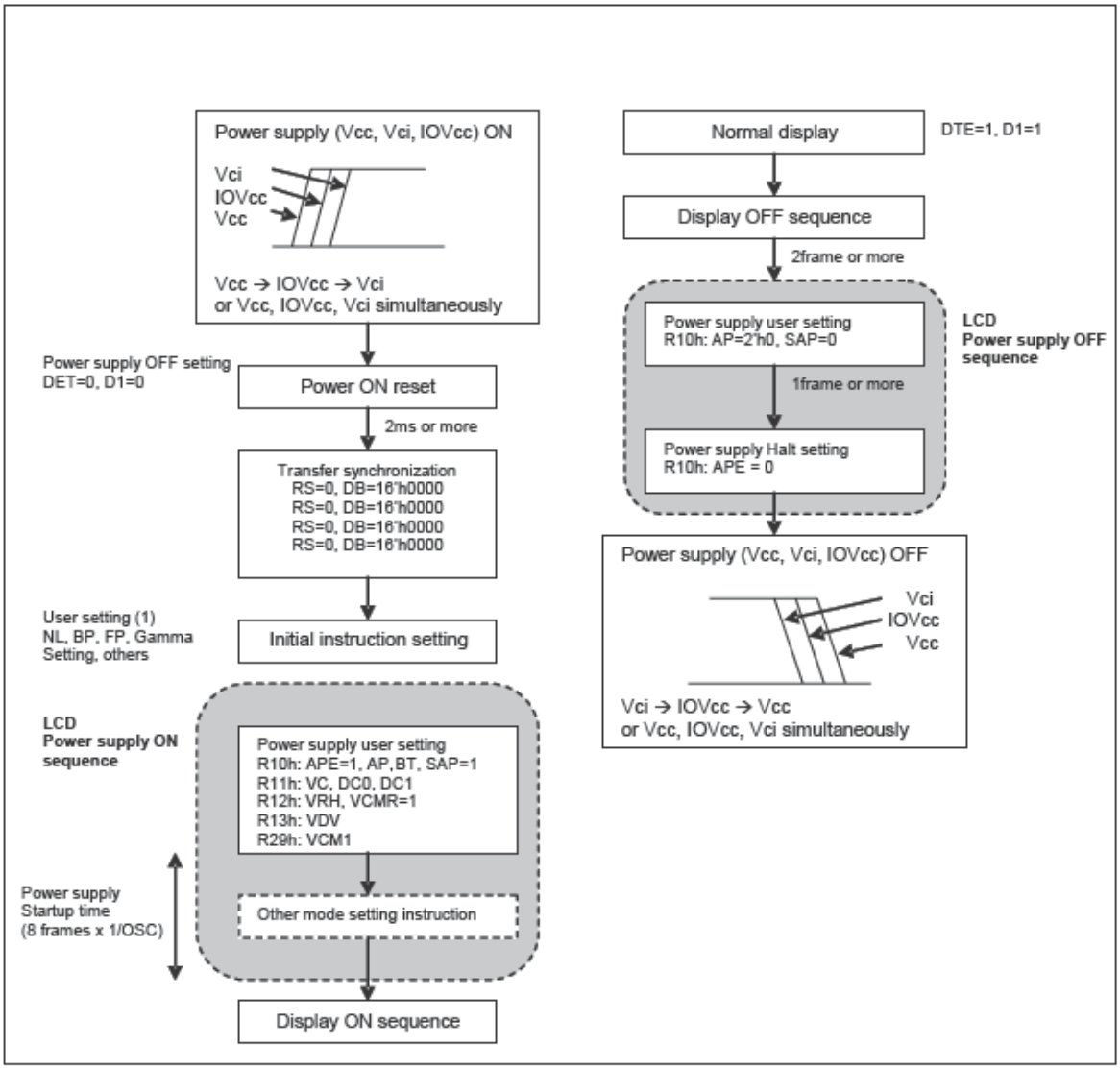
8-1 Display ON / OFF



8-2 Sequence to exit sleep mode



8-3 Power Supply Configuration

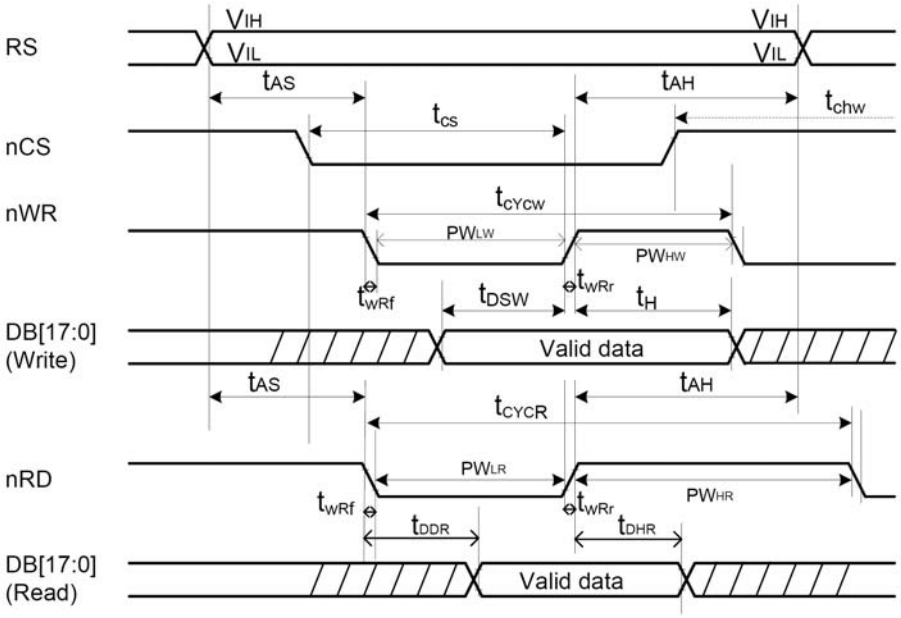


Power Supply ON/OFF Sequence

9 Electrical Characteristics

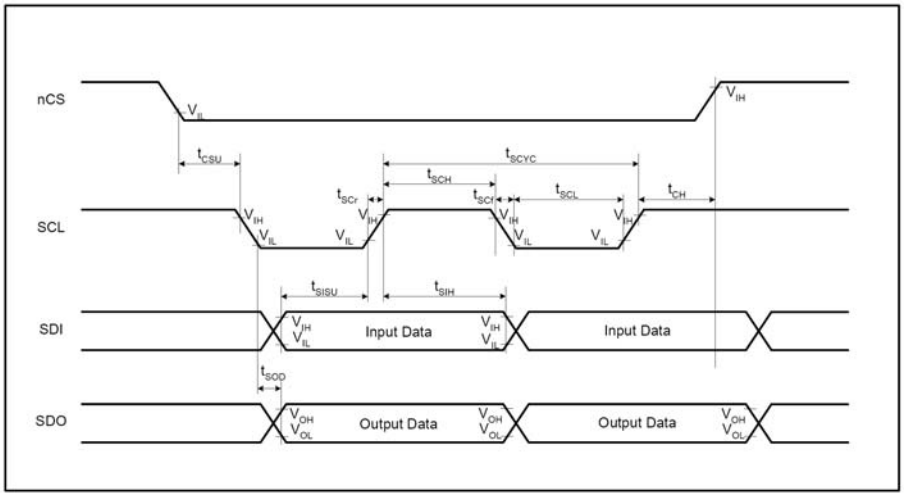
Normal Write Mode (IOVCC = 1.65~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	TBD	-		-
	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	TBD	-	500	-
Write high-level pulse width		PW_{HW}	ns	TBD	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5	-	-	
Write data set up time		t_{DSW}	ns	10	-	-	
Write data hold time		t_H	ns	15	-	-	
Read data delay time		t_{DDR}	ns	-	-	100	
Read data hold time		t_{DHR}	ns	5	-	-	



(IOVCC= 1.65 ~ 3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	μs	TBD	-	-	
	Read (transmitted)	t_{SCYC}	μs	200	-	-	
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	
	Read (transmitted)	t_{SCH}	ns	100	-	-	
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	
	Read (transmitted)	t_{SCL}	ns	100	-	-	
Serial clock rise / fall time		t_{SCr}, t_{SCf}	ns	-	-	5	
Chip select set up time		t_{CSU}	ns	10	-	-	
Chip select hold time		t_{CH}	ns	50	-	-	
Serial input data set up time		t_{SISU}	ns	20	-	-	
Serial input data hold time		t_{SIH}	ns	20	-	-	
Serial output data set up time		t_{SOD}	ns	-	-	100	
Serial output data hold time		t_{SOH}	ns	5	-	-	

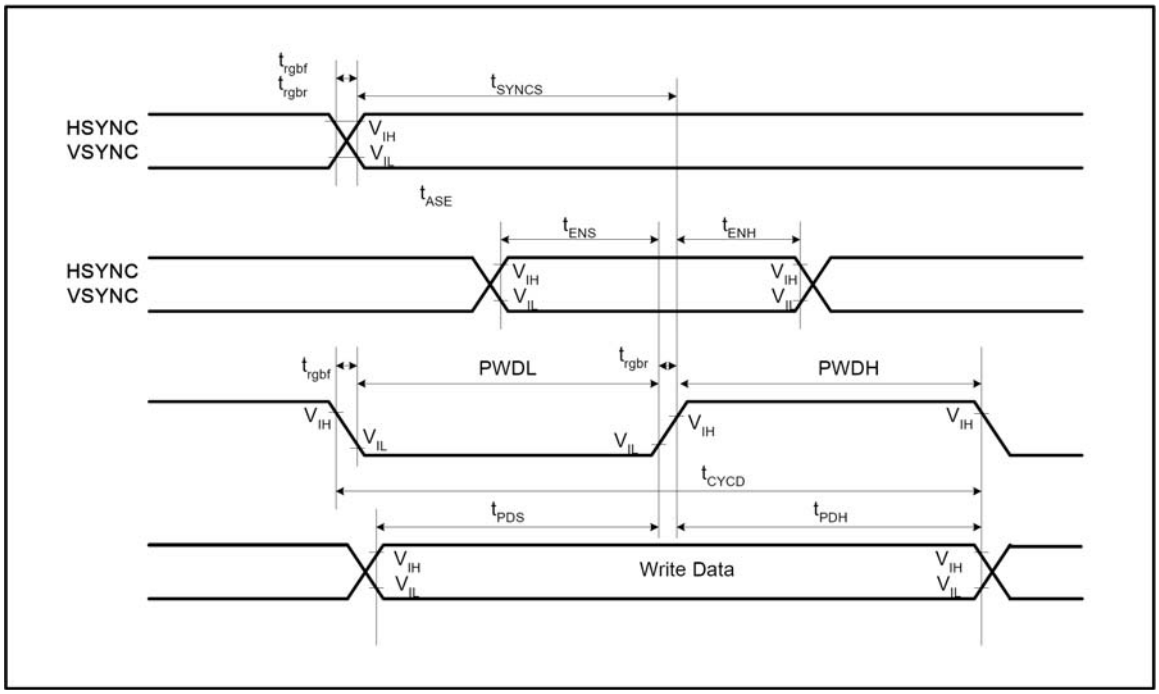


18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	TBD	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-



10 QUALITY AND RELIABILITY

10-1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

10-2 SAMPLING PLAN

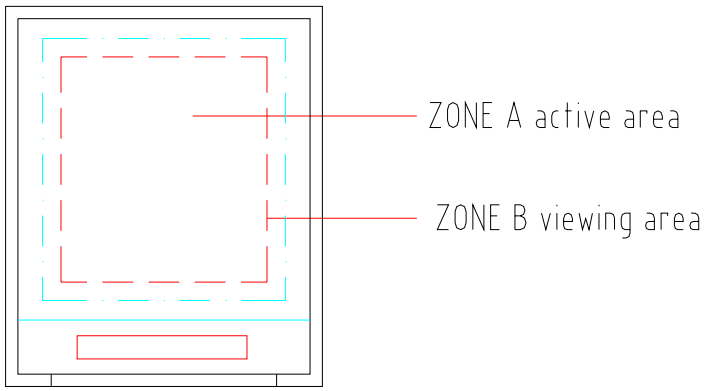
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10-3 ACCEPTABLE QUALITY LEVEL

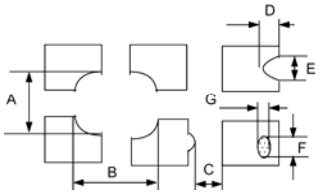
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10-4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under florescent light. The inspection area of LCD panel shall be within the range of following limits.



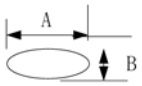
10-5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Class of Defec</th><th>Acceptable level</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td><td>0.65</td></tr>
<tr><td>2</td><td>Scratch,Dent of Plastic Mold</td><td>Serious one is not allowed</td><td>Major</td><td>0.65</td></tr>
<tr><td>3</td><td>Scratch on FPC</td><td>By limited sample</td><td>Major</td><td>0.65</td></tr>
<tr><td>4</td><td>Dot Defect</td><td><table><tr><th>Item</th><th>Number</th></tr><tr><td>Bright dot defect</td><td>N ≦ 0</td></tr><tr><td>Black dot defect</td><td>N ≦ 2</td></tr><tr><td>Total</td><td>N ≦ 2</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
<tr><td>5</td><td>Line Defect</td><td>None</td><td>Minor</td><td>1.5</td></tr>
<tr><td>6</td><td>Uneven Brightness : Line Shape</td><td>None</td><td>Major</td><td>0.65</td></tr>
<tr><td>7</td><td>Uneven Brightness : Dot Shape</td><td>None</td><td>Major</td><td>0.65</td></tr>
<tr><td>8</td><td>Display pattern</td><td> 

Unit:mm
<table><tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr></table>
Note: 1. Acceptable up to 3 damages
2. NG if there're to two or more pinholes per dot</td><td>Minor</td><td>1.5</td></tr>
<tr><td>9</td><td>Scratch of Polarizer :Dot Shape s
Size:
$D = \frac{A+B}{2}$</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.1
0.1 < D ≤ 0.3
0.3 < D</td><td>Ignore
3
0</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
</table>

<table>
<tr>
<td>10</td>
<td>Scratch of Polarizer :

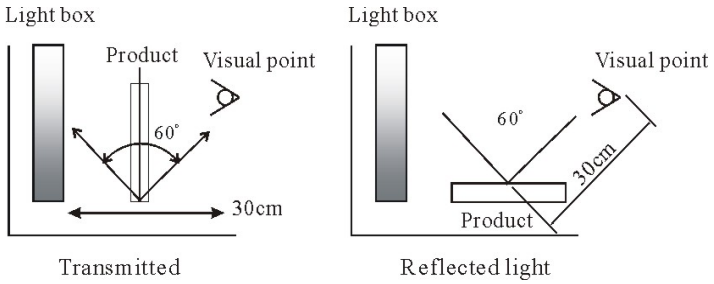
Line Shape

  </td>
<td>
<table>
<tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr>
<tr><td>W≤0.05</td><td>L ≤ 0.3</td><td>Ignore</td></tr>
<tr><td>0.1<W≤0.05</td><td>0.3 < L ≤ 2.0</td><td>N≦3.</td></tr>
<tr><td>0.1<W</td><td>-</td><td>See dot shape</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>11</td>
<td>Bubble in polarizer</td>
<td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.3</td><td>Ignore</td></tr>
<tr><td>0.30 < D ≤ 0.50</td><td>1</td></tr>
<tr><td>0.50 < D</td><td>0</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>12</td>
<td>Stains inclusion : Line shape</td>
<td>
<table>
<tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr>
<tr><td>W≤0.04</td><td>Ignore</td><td>Not Allowed</td></tr>
<tr><td>0.04<W≤0.06</td><td>L ≤ 0.8</td><td>Not Allowed</td></tr>
<tr><td>0.06<W</td><td>-</td><td>Not Allowed</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>13</td>
<td>Stains inclusion : dot shape</td>
<td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.1</td><td>Not Allowed</td></tr>
<tr><td>0.1 < D ≤ 0.2</td><td>Not Allowed</td></tr>
<tr><td>0.25< D</td><td>Not Allowed</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>14</td>
<td>Newton Ring</td>
<td>(A). The lightness of environment is 500 Lux

(B). The distance between product and eye is about 30cm

(C). The angle of 60° between eye

(D). Please find data below for your reference

Not Allowed Newton Ring</td>
<td>Major</td>
<td>0.65</td>
</tr>
</table>

10-6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=72 hrs	
Low Temperature Operation	-10±3°C , t=72 hrs	
High Temperature Storage	80±3°C , t=72hrs	1,2
Low Temperature Storage	-30±3°C , t=72 hrs	1,2
Temperature /Humidity Storage Test	60°C, Humidity 90%, 72 hrs	1,2
Temperature /Humidity Operation Test	40°C, Humidity 90%, 72 hrs	1,2
Thermal Shock Test	-20°C ~ 70°C 60 min 60 min. (1 cycle) Total 20 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge ±5kV, 10times contact discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11 USE PRECAUTIONS

11-1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11-2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

11-3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11-4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that

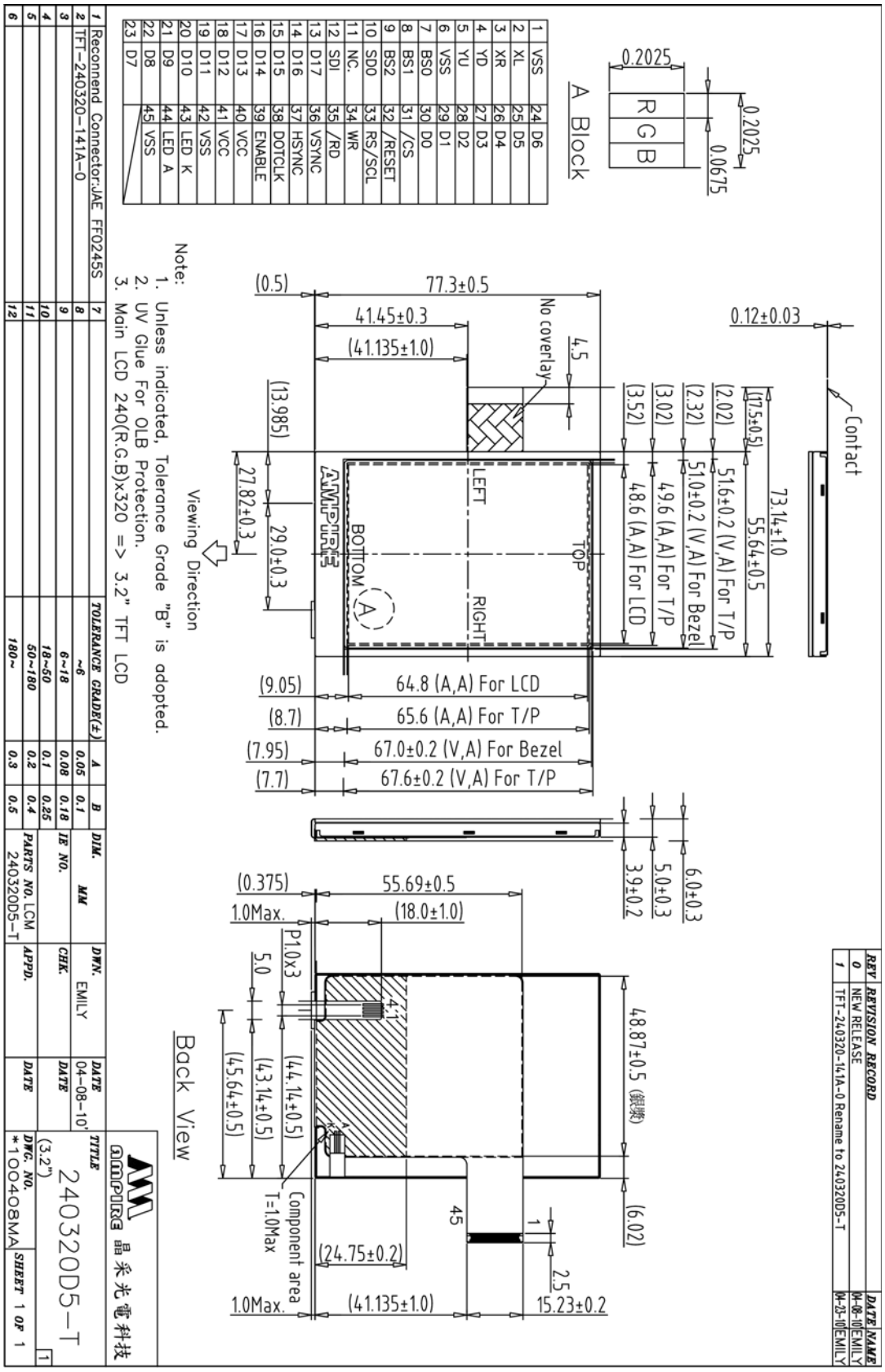
they are shielded from light emissions.

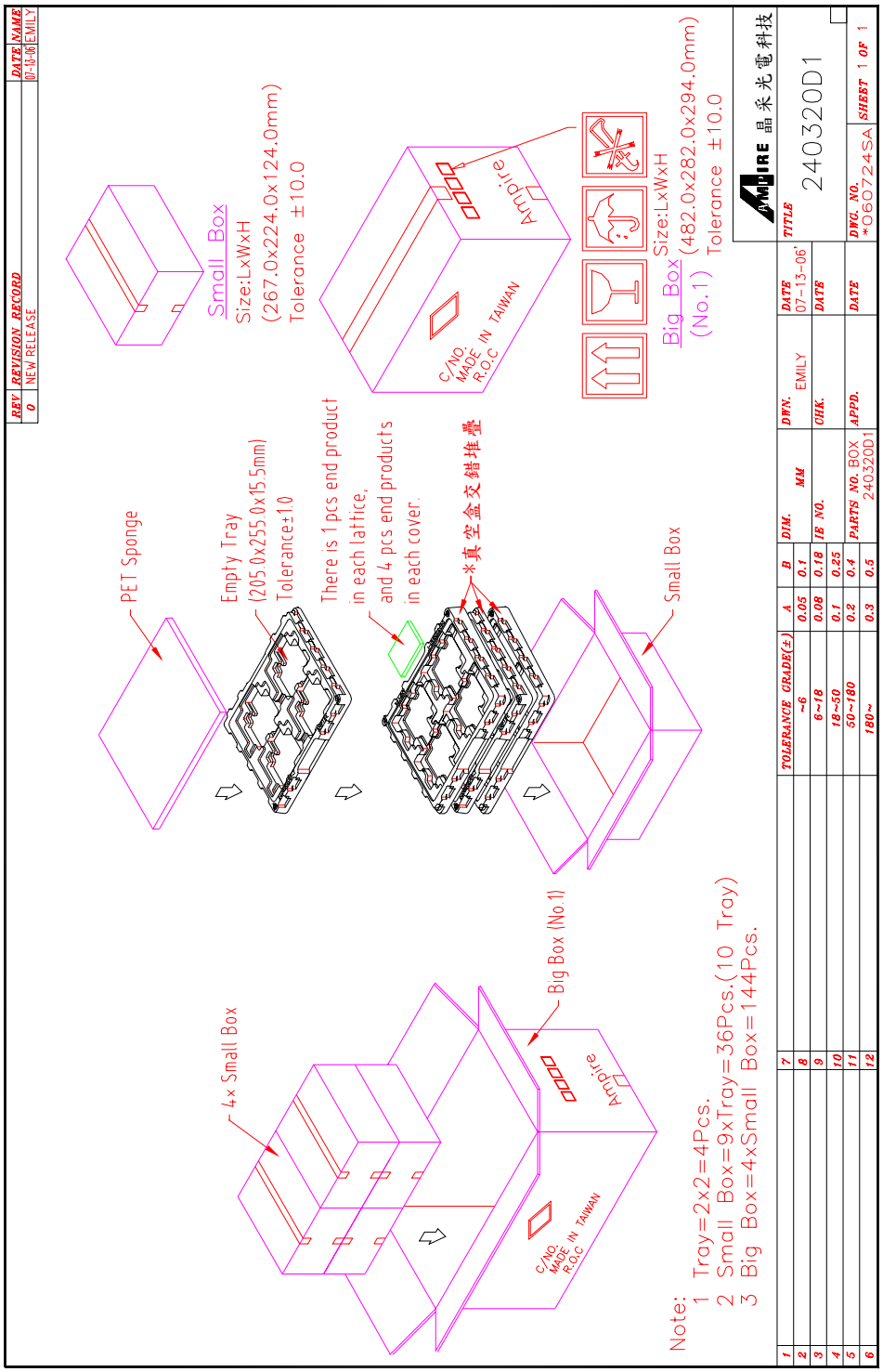
8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

11-5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one years warrantee for all products and three months warrantee for all repairing products.

12 MECHANICAL DRAWING




Small Box
Size:LxWxH
(267.0x224.0x124.0mm)
Tolerance ±10.0
Big Box
Size:LxWxH
(482.0x282.0x294.0mm)
(No.1) Tolerance ±10.0
PET Sponge
Empty Tray
(205.0x255.0x15.5mm)
Tolerance±1.0
There is 1 pcs end product
in each lattice,
and 4 pcs end products
in each cover.
*真空盒交錯堆疊
Small Box
4x Small Box
Big Box (No.1)
Note:
1 Tray=2x2=4Pcs.
2 Small Box=9xTray=36Pcs.(10 Tray)
3 Big Box=4xSmall Box=144Pcs.
REV. REVISION RECORD
0 NEW RELEASE
DATE NAME
07-13-06 EMILY
DWN. EMILY
CHK.
APPD.
DATE 07-13-06'
TITLE
240320D1
DWG. NO. *060724SA
SHEET 1 OF 1
PARTS NO. BOX 240320D1
TOLERANCE GRADE(±)
~6 0.05 0.1
6~18 0.08 0.18
18~50 0.1 0.25
50~180 0.2 0.4
180~ 0.3 0.5