晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS　FOR
LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	**AM-1280480ATMQW-02H**
APPROVED　BY	
DATE	

☐**Approved For Specifications**
☐Approved For Specifications & Sample

AMPIRE CO., LTD.
4F., No.116, Sec. 1, Xintai 5th Rd., Xizhi Dist., New Taipei City 221, Taiwan (R.O.C.)
22181 新北市 汐止區 新台五路一段 116 號 4 樓(東方科學園區 A 棟)
TEL:886-2-26967269 , FAX:886-2-26967196 or 26967270

APPROVED BY	CHECKED BY	ORGANIZED BY

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2014/10/28	--	New Release	KOKAI

1. INTRODUCTION

12.3 inch TFT Liquid Crystal Display module is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller IC on TFT Panel, PCBA, White LED Back-light . This TFT LCD has a 12.3-inch diagonally measured active display area with 1280 horizontal by 480 vertical pixel array resolution.

1.1. The PCBA is an interface board for Ampire 12.3" 1280x480 LCD module.
 Include the following Circuit:

- LVDS Receiver IC: Input 18bit LVDS signal to 18 bit TTL RGB.
- LED driver : Host can turn on the LED Back-light and control the LED brightness.
- MCU : Setting the register value of the T-COM IC and control the power on sequence.
- TFT power circuit: Generate the all the necessary TFT power voltage.
- Optional connector for control the Cap Touch Key and ambient light sensor.

2. PHYSICAL SPECIFICATIONS

Item	Specifications	Remark
LCD size	12.3 inch(Diagonal)	
Apsect ratio	8:3	
Driver element	Active matrix TFT in LTPS technology	
Display resolution	1280 (W) × 3 (RGB) x 480 (H) dots	
Display mode	Normally White, Transmissive	
Pixel Size	0.228 (W) x0.228 (H) mm	
Active area	291.84 (W) x 109.44 (H) mm	
Color arrangement	R.G.B-stripe	
Interface	LVDS	

3. ABSOLUTE MAX. RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Supply voltage range	VDD	-0.3	4	V	(1)
LED Driver Supply voltage range	VLED	-0.3	12.5	V	(1)
Voltage range at any terminal	VI	-0.3	VDD + 0.3	V	
Operating Temperature	Top	-30	+85	℃	
Storage Temperature	Tstg	-40	+90	℃	

Note : All voltage values are with respect to the GND   terminals unless otherwise noted.

4. ELECTRICAL CHARACTERISTICS

4.1. Power Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Logic Supply Voltage	VDD	3.0	3.3	3.6	V	
LED driver supply voltage	VLED	5.0	12.0	12.2	V	
VDD Current	IDD	--	(175)	--	mA	(1)
LVDS DRIVER DC SPECIFICATIONS						
Differential Output Voltage	VOD	250	350	450	mV	RL=100ohm
Change in VOD between Complimentary Output States	ΔVOD	--	--	35	mV	RL=100ohm
Common Mode Voltage	VOC	1.125	1.25	1.375	V	RL=100ohm
Change in VOC between Complimentary Output States	ΔVOC	--	--	35	mV	RL=100ohm
LVDS RECEIVER DC SPECIFICATIONS						
Differential Input High Threshold	VTH	--	--	+100	mV	VOC=+1.2V
Differential Input Low Threshold	VTL	-100	--	--	mV	VOC=+1.2V

Note1: Ta=25℃ , Display pattern : All Black

4.2. LED BACKLIGHT DRIVER UNIT

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Voltage	VLED	5	12	12.2	V	
Input Current	ILED	--	850	--	mA	100% PWM duty
ADJFrequency	Fpwm	100		200	Hz	
LED Forward Current	IF	--	600	--	mA	Ta=25°C
LED Forward Voltage	VF		12.8		V	IF=600mA, Ta=25°C

Note 1: Ta means ambient temperature of TFT-LCD module.

Note 2: VLED, ILED are defined for LED B/L. (100% duty of PWM dimming)

Note 3: IF, VF, Fpwm are defined for LED Driver.

Note 4: If the module is driven by high current or at high ambient temperature & humidity condition. The operating life will be reduced.

Note 5: the structure of LED B/L shows as below.
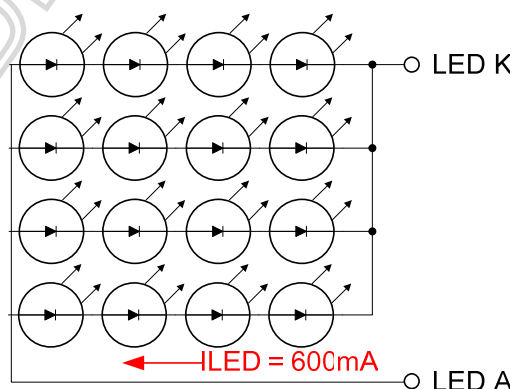
PWM Dimming Control
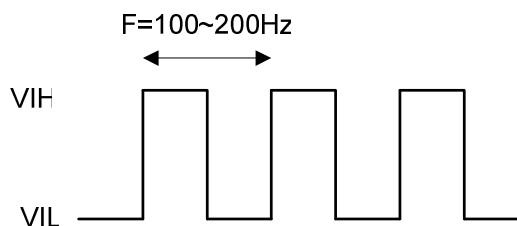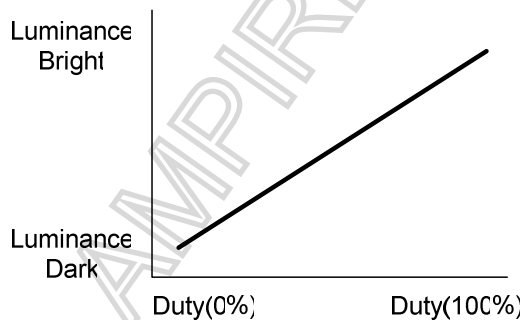
5. Optical Specifications

Item	Symbol	Condition	Values Min	Values Typ	Values Max	Unit	Remark
Viewing angle (CR≥ 10)	θ_L	θ=180°(9 o'clock)	55	60	-	degree	Note 1
	θ_R	θ=0°(3 o'clock)	55	60	-		
	θ_T	θ=90°(12 o'clock)	50	55	-		
	θ_B	θ=270°(6 o'clock)	50	55	-		
Response time	T_{ON}		-	15	20	Msec	Note 2
	T_{OFF}			5	8		Note 3
Contrast ratio	CR		300	500	-	-	Note 4
Color chromaticity	W_X	Normal θ=Φ=0°	0.26	0.31	0.36	-	Note 2
	W_Y		0.28	0.33	0.38	-	Note 5 Note 6
Luminance	L		800	1000		cd/m^2	Note 6
Luminance uniformity	Y_U		70	80	-	%	Note 7
NTSC	-	-	-	50	-	%	

Test Conditions:

1. VDD=3.3V, IL=600 mA (Backlight current), the ambient temperature is 25℃.

2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range

Fig. 6-1 Definition of viewing angle
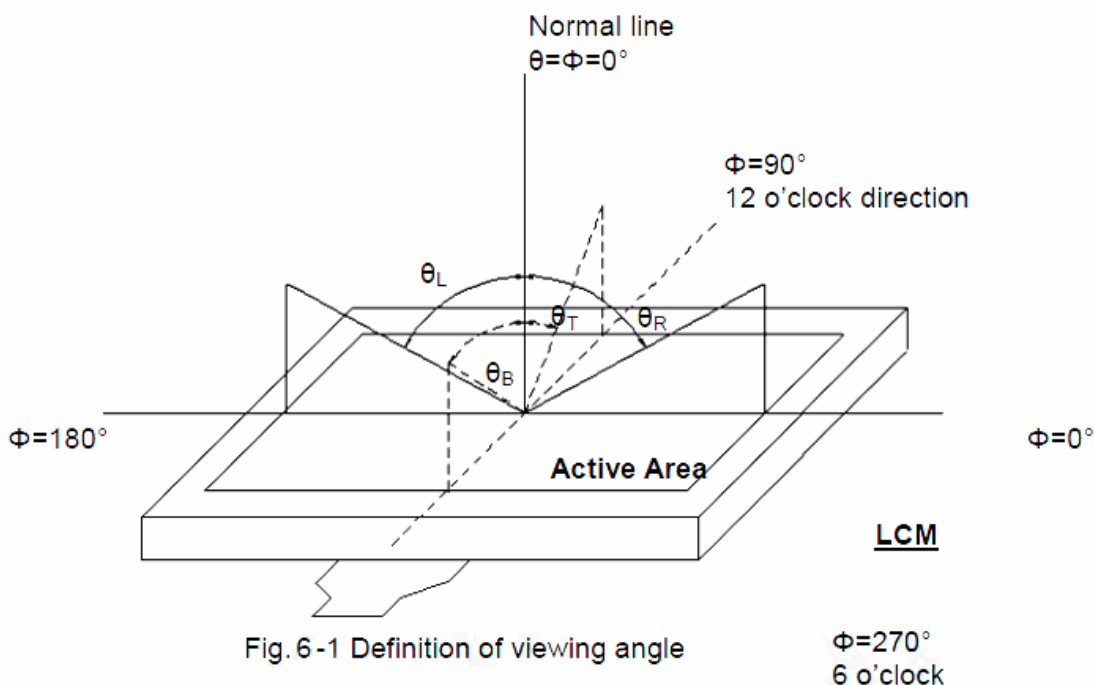
Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by ELDIM-EZ contrast/Height :1.2mm, Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/ Field of view: 1°/Height: 500mm .)
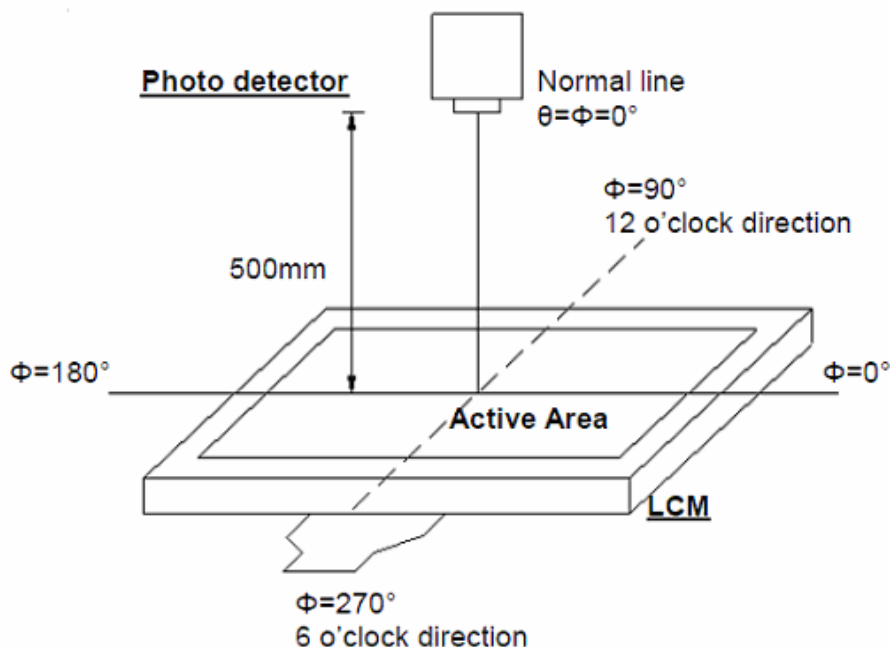
Fig. 6-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.
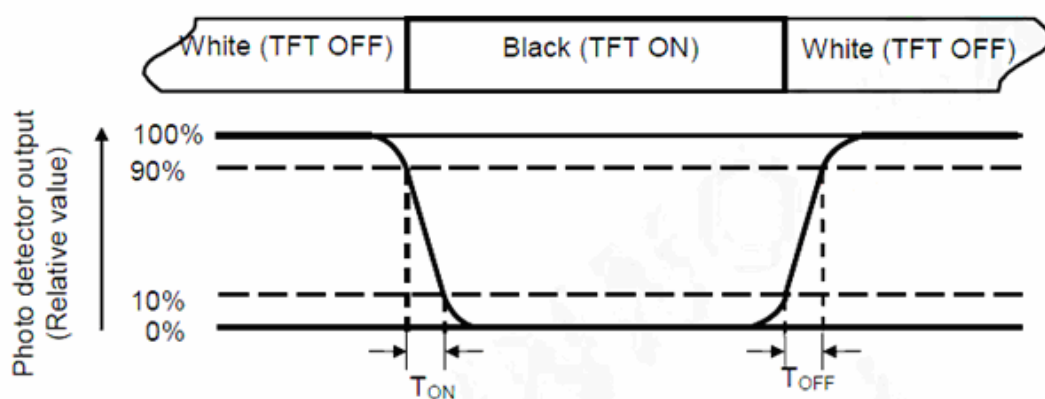
Fig. 6-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness @ "White" state}}{\text{Brightness @ "Black" state}}$$
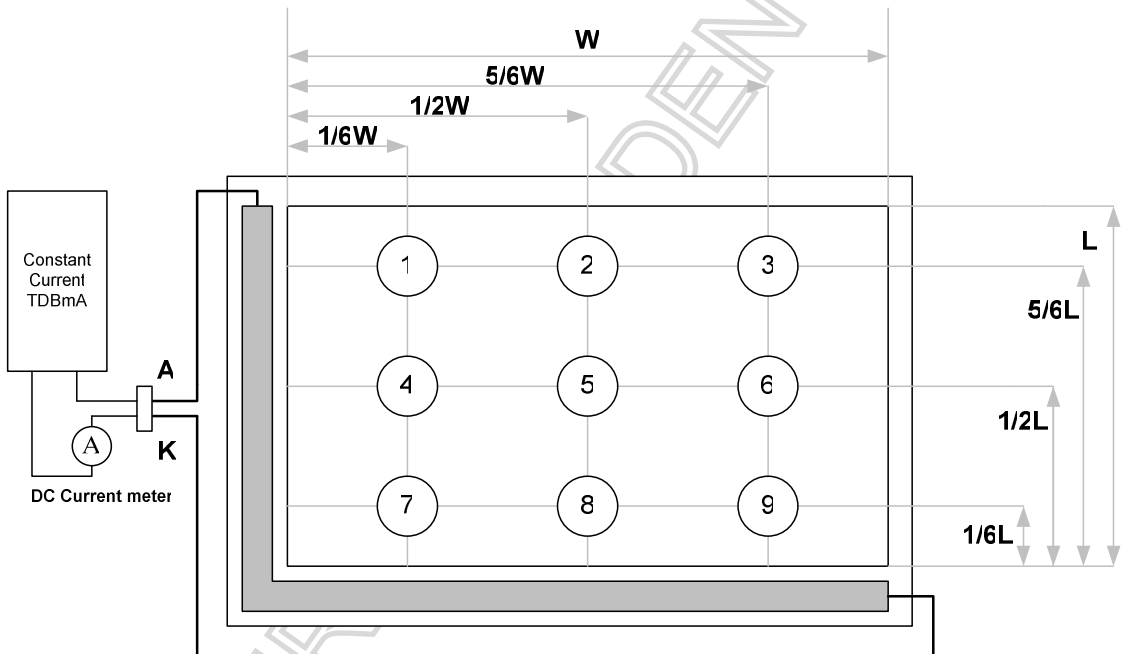
Note 5: Definition of color chromaticity (CIE1931)

      Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the

      panel. The LED driving condition is IL=600 mA.

Note 7: Definition of Luminance Uniformity

$$\text{Luminance Uniformity (Yu)} = \frac{B_{min}}{B_{max}}$$

B_{max}: The measured maximum luminance of all measurement position.

B_{min}: The measured minimum luminance of all measurement position.

6. INTERFACE

6.1. CN1: LVDS INTERFACE CN1: HRS DF19G-20P-1H or Equivalent

Pin No.	Symbol	I/O	Description	Note
1	VDD	P	Power supply for digital circuit (3.3V)	
2	VDD	P	Power supply for digital circuit (3.3V)	
3	GND	P	Power ground	
4	GND	P	Power ground	
5	IN0-	I	LVDS receiver negative signal channel 0	
6	IN0+	I	LVDS receiver positive signal channel 0	
7	GND	P	Power ground	
8	IN1-	I	LVDS receiver negative signal channel 1	
9	IN1+	I	LVDS receiver positive signal channel 1	
10	GND	P	Power ground	
11	IN2-	I	LVDS receiver negative signal channel 2	
12	IN2+	I	LVDS receiver positive signal channel 2	
13	GND	P	Power ground	
14	CLK-	I	LVDS receiver negative signal clock	
15	CLK+	I	LVDS receiver positive signal clock	
16	GND	P	Power ground	
17	NC	-	No connection	
18	NC	-	No connection	
19	GND	P	Power ground	
20	GND	P	Power ground	

6.2. ZIF connector Pitch 1.0 x 10 Pin

Pin No.	Symbol	I/O	Description	Note
1	VLED	P	Power supply for LED Driver circuit.	
2	VLED	P		
3	GND	P	Power ground	
4	GND	P		
5	ADJ	I	Adjust the LED brightness by PWM	
6	NC	-	No connection	
7	NC	-	No connection	
8	NC	-	No connection	
9	NC	-	No connection	
10	NC	-	No connection	

6.3. CN3 S2B-EH or Equivalent

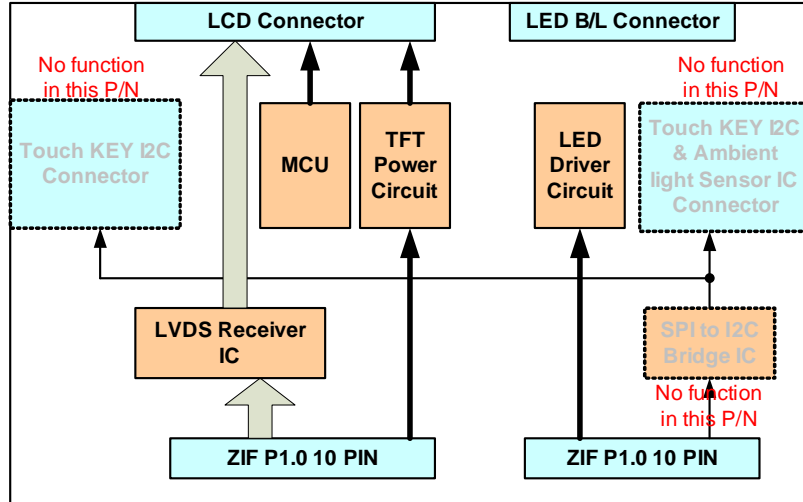| PIN NO.	SIGNAL	LEVEL	FUNCTION
1	VLED	P	Power supply for LED Driver circuit.
2	GND		Heater Power GND

(NoteL: CN2 Pin1,2 and CN3 Pin1 are VLED pin. Internally connected together. Do not supply different voltage at the same time.)

7. BLOCK DIAGRAM

1,2. VDD
3,4. GND
5,6. IN0-,IN0+
7. GND
8,9. IN1-,IN1+
10. GND
11,12. IN2-,IN2+
13. GND
14,15. CLK-,CLK+
16. GND
17,18. NC
19,20. GND

1.VLED
2.VLED
3.GND
4.GND
5.ADJ
6.NC
7.NC
8.NC
9.NC
10.NC

8. LVDS Input Data Format

Note : R/G/B data 5 : MSB, R/G/B data 0 : LSB

Signal Name	Description	Remark
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Date 5 (MSB) Green Date 4 Green Date 3 Green Date 2 Green Date 1 Green Date 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN+ RxCLKIN-	LVDS Clock Input	
DE	Display Enable	
VS	Vertical Sync	
HS	Horizontal Sync	

9. AC Timing characteristic

9.1. AC Timing characteristic of LVDS

Switching Characteristics

Vcc = 3.0 - 3.6V, Ta = -10 - +70 ˚C

RECEIVER

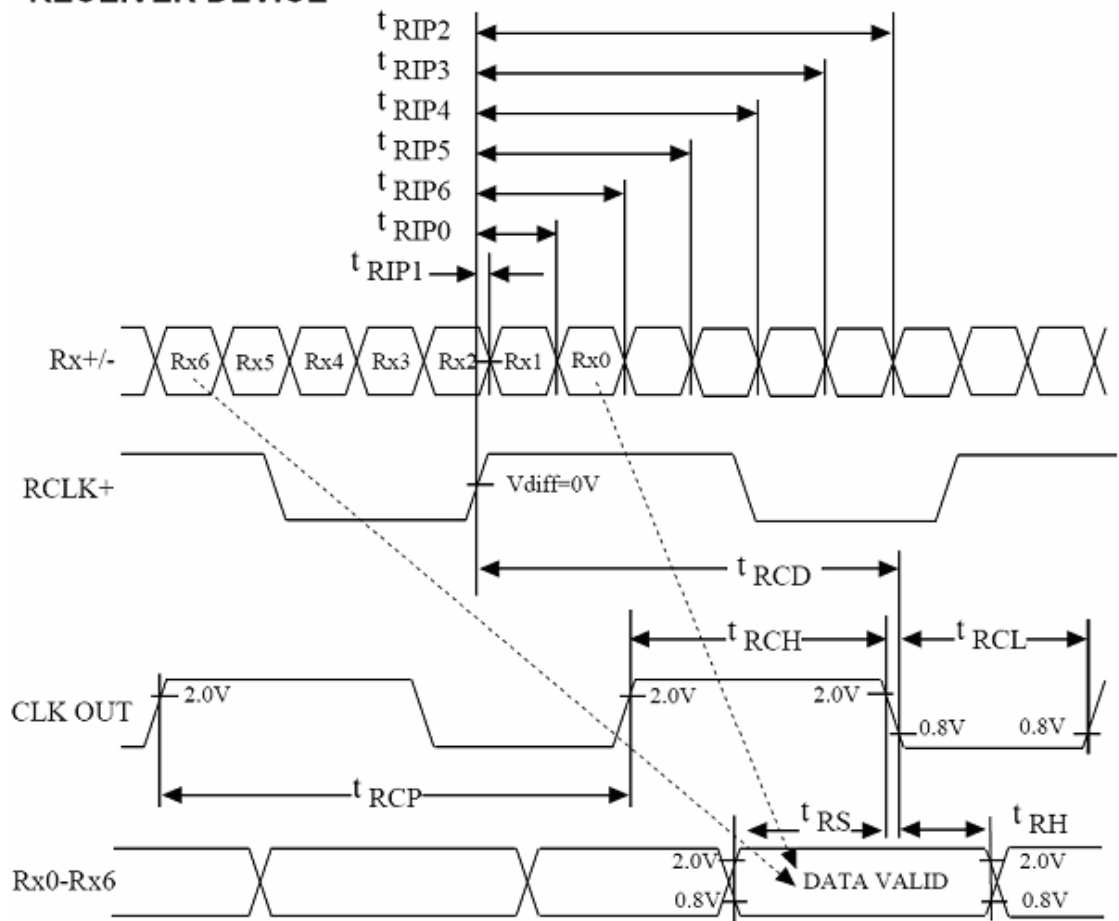|					
t_{RCP}	CLK OUT Period	11.76	T	50.0	ns
t_{RCH}	CLK OUT High Time		4T/7		ns
t_{RCL}	CLK OUT Low Time		3T/7		ns
t_{RCD}	RCLK+/- to CLK OUT Delay		5T/7		ns
t_{RS}	TTL Data Setup to CLK OUT	3T/7-2.5			ns
t_{RH}	TTL Data Hold from CLK OUT	4T/7-3.5			ns
t_{TLH}	TTL Low to High Transition Time		3.0	5.0	ns
t_{THL}	TTL High to Low Transition Time		3.0	5.0	ns
t_{RIP1}	Input Data Position 0 (T=11.76ns)	-0.4	0.0	0.4	ns
t_{RIP0}	Input Data Position 1 (T=11.76ns)	T/7-0.4	T/7	T/7+0.4	ns
t_{RIP6}	Input Data Position 2 (T=11.76ns)	2T/7-0.4	2T/7	2T/7+0.4	ns
t_{RIP5}	Input Data Position 3 (T=11.76ns)	3T/7-0.4	3T/7	3T/7+0.4	ns
t_{RIP4}	Input Data Position 4 (T=11.76ns)	4T/7-0.4	4T/7	4T/7+0.4	ns
t_{RIP3}	Input Data Position 5 (T=11.76ns)	5T/7-0.4	5T/7	5T/7+0.4	ns
t_{RIP2}	Input Data Position 6 (T=11.76ns)	6T/7-0.4	6T/7	6T/7+0.4	ns
t_{RPLL}	Phase Lock Loop Set			10.0	ms

RECEIVER DEVICE

Note:
1) Vdiff = (RA+) - (RA-), ... (RCLK+) - (RCLK-)

9.2. Timing characteristic of Panel
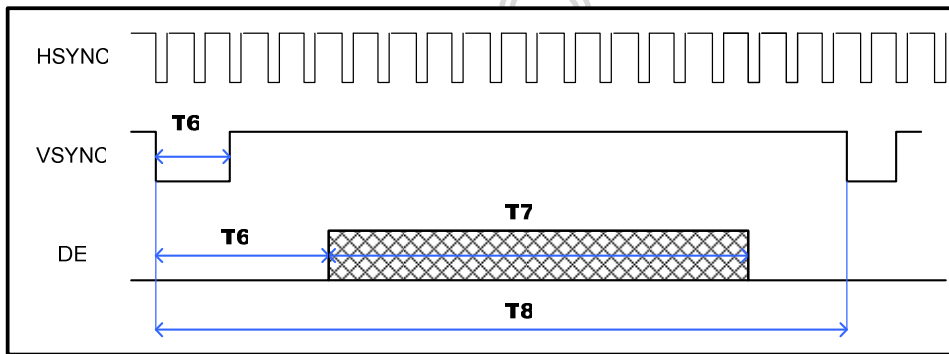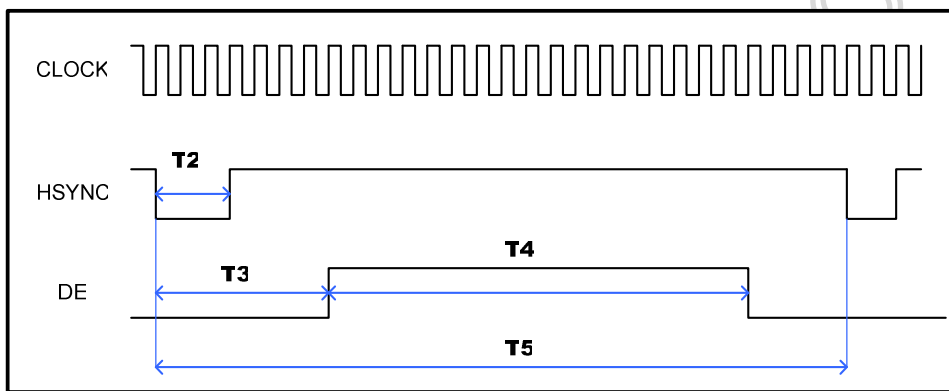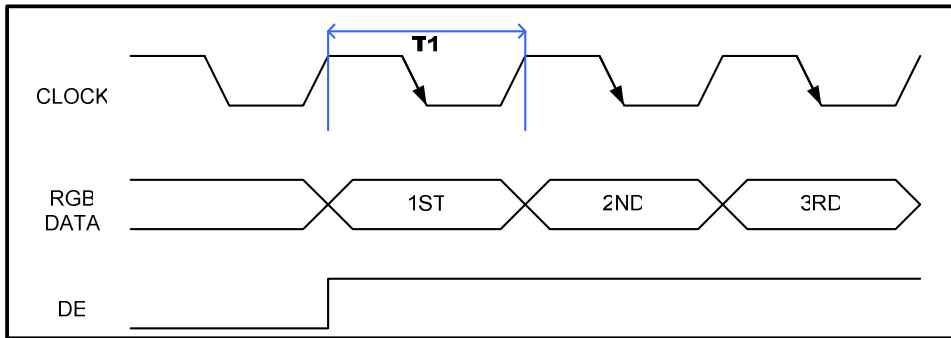
HPW=5 ; HBP=16 ; HFP=70 , VPW=1,VBP=3,VFP=18

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Clock Frequency	1/T1	31.26	41.34	43	MHz
HSYNC Plus Wide	T2		5		clocks
HSYNC to DE	T3		16		Clocks
Horizontal Display Period	T4		1280		Clocks
Horizontal total Period	T5		1366		Clocks
VSYNC Plus Wide	T2		1		Lines
VSYNC to DE	T6		3		Lines
Vertical Display Period	T7		480		Lines
Vertical total Period	T8		501		Lines

9.3. Power ON/OFF Timing

Symbol	Value			Unit
	Min.	Typ.	Max.	
T1	0.5	--	2	us
T2	0	20	30	ms
T3	200	--	--	ms
T4	200	--	--	ms
T5	0	20	30	ms
T6	0.5	--	2	us
T7	1000	--	--	ms

10. OUTLINE DIMENSION

Preliminary

The contents of this document are confidential and must not be disclosed wholly or in part to any third part without the prior written consent of AMPIRE CO., LTD

Back View

Note:
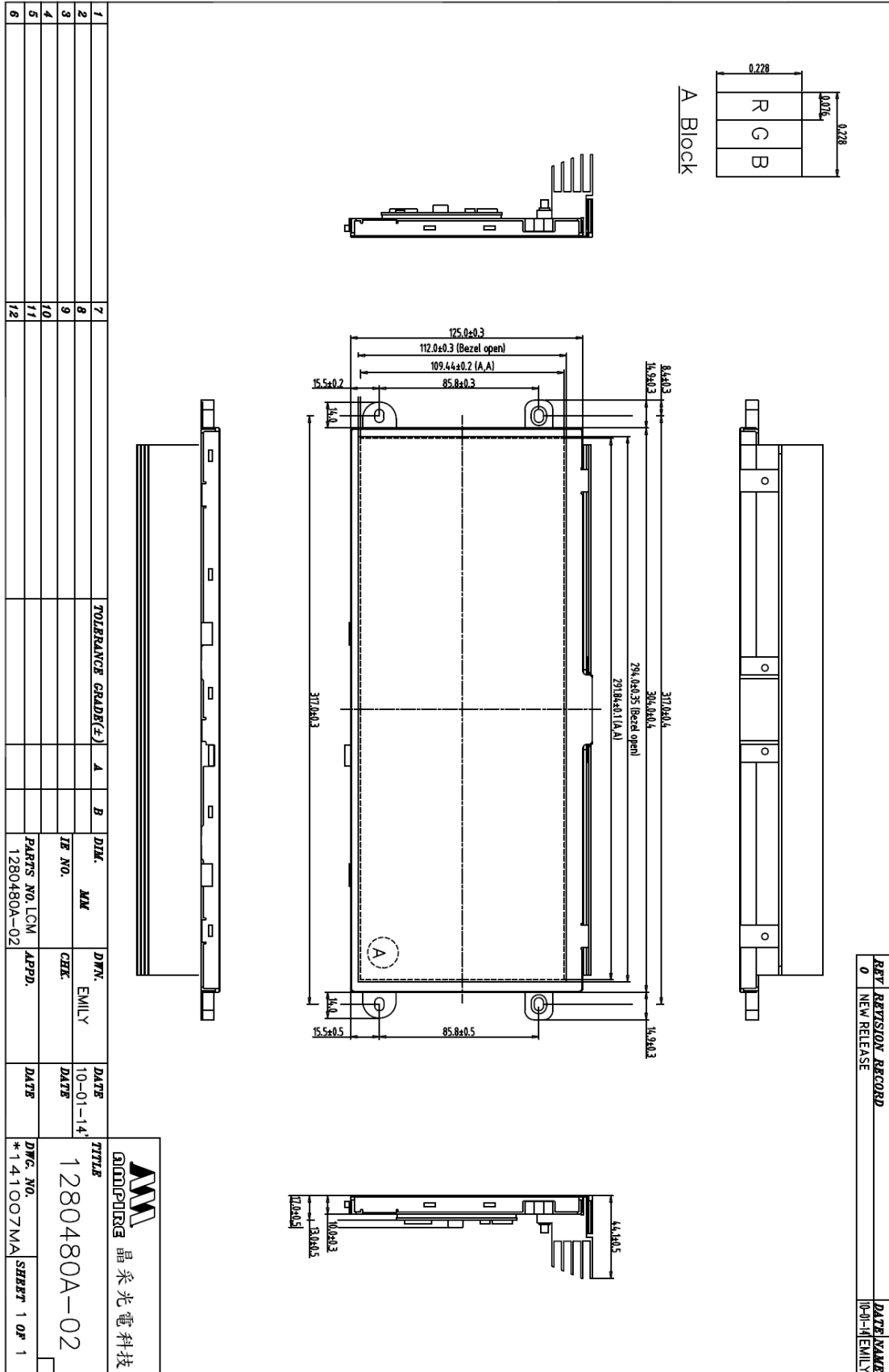1. Unless indicated, Tolerance "±0.5"
2. UV Glue For OLB Protection.
3. CN1:P1.0 20PIN/CP100-S20G-H16 or Equivalent
4. CN2:P1.0 10PIN/106H10-011001-T1-R or Equivalent
5. CN7:DIP P2.5X2PIN 90° MPHRF-102TTW717 or Equivalent
6. LCD 1280X3(R.G.B)x480=> 12.3" Digital TFT LCD

CN7

1	VLED
2	GND

CN2

1	VLED
2	VLED
3	GND
4	GND
5	ADJ
6	NC
7	NC
8	NC
9	NC
10	NC

CN1

11	RX2-
12	RX2+
13	GND
14	CLK-
15	CLK+
16	GND
17	NC
18	NC
19	GND
20	GND

1	VDD
2	VDD
3	GND
4	GND
5	IN0-
6	IN0+
7	GND
8	IN1-
9	IN1+
10	GND

TOLERANCE GRADE(±)	A	B	DIM.

REV. REVISION RECORD | DATE NAME
0 NEW RELEASE | 10-01-14 EMILY

TITLE: 1280480A-02

PARTS NO.LCM-1 1280480A-02

DWN. EMILY DATE 10-01-14

DWG. NO. *141008MA SHEET 1 OF 1

AMPIRE 晶采光電科技