## WINSTAR Display

# **OLED SPECIFICATION**

Model No:

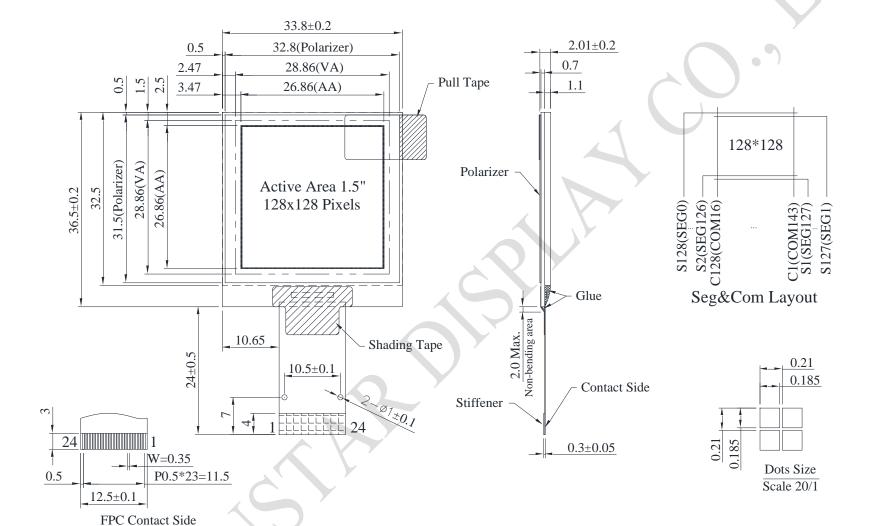
WEO128128H

# **General Specification**

Item	Dimension	Unit	
Dot Matrix	128 x 128 Dots	- ^	
Module dimension	33.80 x 36.50 x 2.01	mm	
Active Area	26.86 x 26.86	mm	
Pixel Size	0.185 x 0.185	mm	
Pixel Pitch	0.210 x 0.210	mm	
Display Mode	Passive Matrix		
Display Color	Monochrome		
Drive Duty	1/128 Duty		
Gray Scale	4 bits		
IC	CH1120		
Interface	8080,SPI,I2C		
Size	1.5 inch		

**WEO128128H** 第 2 頁 · 共 4 頁

#### **Contour Drawing & Block Diagram**



PIN SYMBOL		
1	ESD_GND	
2	VPP	
3	VCOMH	
4	VDD	
5	NC	
6	IM1	
7	IM2	
8	VSS	
9	IREF	
10	CSB	
11	RESB	
12	A0	
13	WRB	
14	RDB	
15	D0	
16	D1	
17	D2	
18	D3	
19	D4	
20	D5	
21	D6	
22	D7	
23	VPP	
24	ESD_GND	

The non-specified tolerance of dimension is  $\pm 0.3\ mm$  .

Scale 1/1

## **Interface Pin Function**

No.	Symbol	Function				
1	ESD_GND	This pin should be connected to GND.				
2	VPP	This is the most positive voltage supply pin of the chip. It should be supplied externally.				
3	VCOMH	This is a pin for the voltage output high level for common signals.  A capacitor should be connected between this pin and GND.				
4	VDD	Power s	upply for logic			
5	NC	No conn	ection			
	15.44	These a		rface mode sele		
6	IM1		8080	3-wire SPI	4-wire SPI	I2C
		IM1	1	0	0	1
7	IM2	IM2	1	1	0	0
		These p	ins must be con	nected to "H" or	"L".	
8	VSS	Ground for logic and analog. This pin should be connected to GND externally.				ed to GND
9	IREF	This is a segment current reference pin. A resistor should be connected between this pin and GND.				ID.
10	CSB	This pin is the chip select input. When CSB = "L", then the chip select becomes active, and data/command I/O is enabled. When in I2C interface, this pin is not used, so it must be connected to "L".				
11	RESB	This is a reset signal input pin. When RESB is set to "L", the settings are initialized. The reset operation is performed by the RESB signal level. This pin internal pull high.				
12	A0	This is the Data/Command control pin that determines whether the data bits are data or a command.  A0 = "H": the inputs at D0 to D7 are treated as display data.  A0 = "L": the inputs at D0 to D7 are transferred to the command registers.  In I2C interface, this pin serves as SA0 to distinguish the different address of OLED driver.  When in 3-wire interface, this pin is not used, so it must be connected to "L".				
13	WRB	When co to the 80 the rising When in	080 MPU WR sig g edge of the W	080 MPU, this is gnal. The signals	on the data bus	

**\*\* WINSTAR** WEO128128H 第4頁·共4頁

14	RDB	This is a MPU interface input pin. When connected to an 8080 series MPU, it is active LOW. This pin is connected to the RD signal of the 8080 series MPU, and the data bus is in an output status when this signal is "L".  When in 3-wire.4-wire & I2C interface, this pin is not used, so it must be connected to "L".
15	D0	
16	D1	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit
17	D2	standard MPU data bus.
18	D3	When the serial interface(SPI) and I2C is selected, then D0 serves as the
19	D4	serial clock input pin (SCL) and D1 serves as the serial data input pin (SI). At
20	D5	this time, D2 to D7 are set to high impedance. D7~D2 is recommended to
21	D6	connect the VDD or GND. It is also allowed to leave D7~D2 unconnected.
22	D7	
23	VPP	This is the most positive voltage supply pin of the chip. It should be supplied externally.
24	ESD_GND	This pin should be connected to GND.

**WEO128128H** 第 5 頁 · 共 4 頁

## **Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit
Supply Voltage for Logic	VDD	-0.3	3.5	V
Supply Voltage for Display	VPP	-0.3	15.0	V
Operating Temperature	TOP	-40	+80	°C
Storage Temperature	TSTG	-40	+85	°C

#### **Electrical Characteristics**

#### **DC Electrical Characteristics**

Item	Symbol	Condition	Min	Тур	Max	Unit
Supply Voltage for Logic	VDD	-	1.65	3.0	3.3	٧
Supply Voltage for Display	VPP	O-Y	8.0	14.5	15.0	٧
High Level Input	VIH	3 <sup>7</sup>	0.8×VDD	-	VDD	V
Low Level Input	VIL	<u>-</u>	GND	-	0.2×VDD	V
High Level Output	VOH	-	0.8×VDD	-	VDD	V
Low Level Output	VOL	-	GND	-	0.1×VDD	V
Display 50% Pixel on	IPP	VPP =14.5V	-	20	30	mA

**WEO128128H** 第 6 頁 · 共 4 頁