

晶采光電科技股份有限公司 AMPIRE CO., LTD.

Specifications for LCD module

Customer	
Customer part no.	
Ampire part no.	AM-1280800W1TZQW-20H
Approved by	
Date	

- □ Preliminary Specification
- **■** Formal Specification

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This Specification is subject to change without notice.

Date: 2022/11/23 AMPIRE CO., LTD. 1

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2022/09/26 2022/10/31	 12,21,22	New Release Update interface and drawings – modify Pin 31~34 from VLED to NC	Jessica Jessica
2022/11/23	1,21,22	Change to official part-number	Jessica

1. General Descriptions

1.1 Introduction

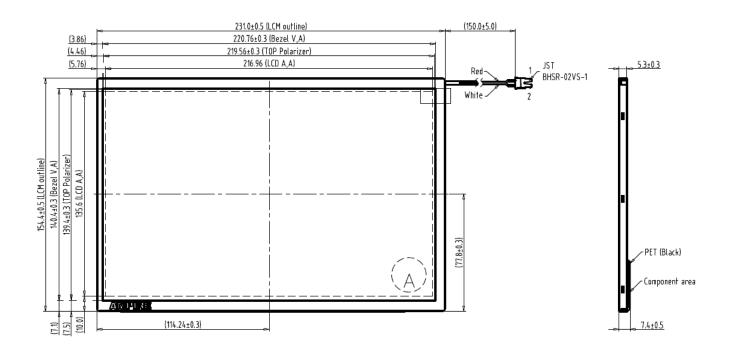
The LCM is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a backlight system, column driver and row driver circuit. This TFT LCD has a 10.1-inch diagonally measured active display area with WXGA resolution (1280 horizontal by 800 vertical pixels array).

1.2 Features

- (1) 10.1" TFT LCD Panel
- (2) LED Backlight System
- (3) Supported WXGA 1280x800 pixels resolution
- (4) MIPI interface

1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	10.1	Inch
Active Area	216.96(H) x 135.6(V)	mm
Pixel Format	1280(RGB) x800	-
Pixel Pitch	0.1695(H)×0.1695 (V)	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally Black	-
White Luminance	500 (Typ.)	cd /m2
Electrical Interface (Logic)	MIPI	-
Support Color	16.7M	-



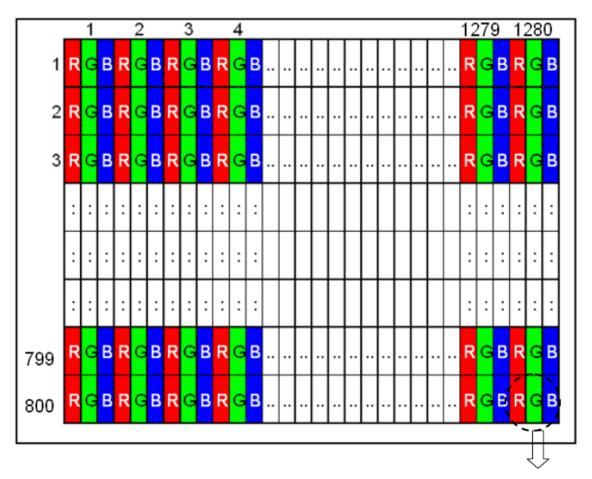
2. Absolute Maximum Ratings

Item	Symbol			Unit	Remark
item	Syllibol	Min.	Max.	Ollit	Remark
Power Voltage	VDD	2.3	3.6	V	VSS=0V, TA=25°ℂ
1 ower venage	VLED	-0.3	24	V	
Operation Temperature	ТОР	-20	70	$^{\circ}\! \mathbb{C}$	
Storage Temperature	TST	-30	80	$^{\circ}\!\mathbb{C}$	

Note(1) The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

3. Pixel Format Image

It shows the relationship of the input signals and LCD pixel format image.



R+G+B dots=1 pixel

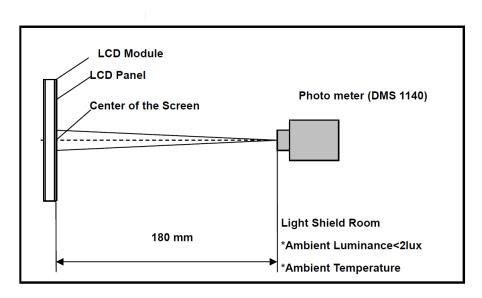
4. Optical Characteristics

The optical characteristics are measured under stable conditions as following notes

Item	Conditions		Min.	Тур.	Max.	Unit	Note
	Horizontal	θL	(75)	(85)	1		
Viewing Angle	ПОПДОПІАІ	θR	(75)	(85)	-	dograa	(4) (2) (2)
(CR>10)	Vertical	ΘТ	(75)	(85)	-	degree	(1),(2),(3)
	verticai	θВ	(75)	(85)	-		
Contrast Ratio	Cente	r	(600)	(800)	-	-	(1),(2),(4)
	Rising	I	-	-	-	ms	
Response Time	Falling)	-	-	-	ms	(1),(2),(5)
	Rising + Falling		-	25	-	ms	
	NTSC		-	45	-	%	(1),(2)
	Red	Х		0.561		-	(1),(2)
	Red	у		0.334		-	
Color	Green	Х		0.341		-	
Chromaticity	Green	у	Тур.	0.568	Тур.	-	
(CIE1931)	Blue	Х	-0.05	0.161	+0.05	-	
	Blue	у		0.129		-	
	White	Х		0.313		-	
	White	у		0.329		-	
White Luminance	Center		400	500	-	cd/m^2	(1),(2),(6)
Luminance Uniformity	9Points		70	75	-	%	(1),(2),(6)

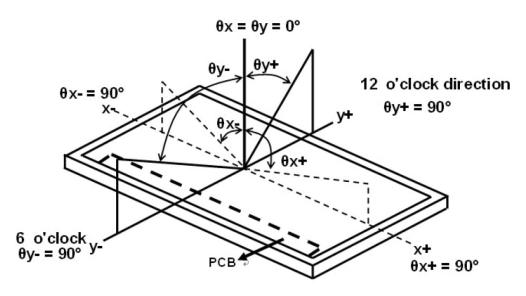
Note(1) Measurement Setup:

The LCD module should be stabilized at given temperature(25°C) for 15 minutes to Avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



Note(2) The LED input parameter setting as: PWM: duty 100 %

Note(3) Definition of viewing angle:



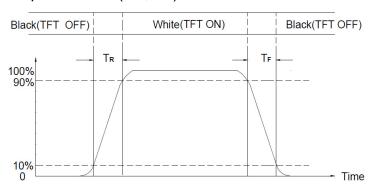
Note(4) Definition of Contrast Ratio (CR)

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The contrast ratio can be calculated by the following expression Contrast Ratio (CR) = L255 / L0

L63: Luminance of gray level 255, L0: Luminance of gray level 0

Note(5) Definition of Response Time (TR, TF)



Note(6) Definition of brightness luminance

Active area is divided into 9 measuring areas (Refer to bellow figure). Every measuring point is placed at the center of each measuring area.

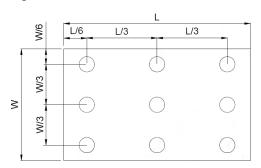
Bmin

Luminance Uniformity (Yu) = _____

Bmax

L ---- Active area length

W ---- Active area width



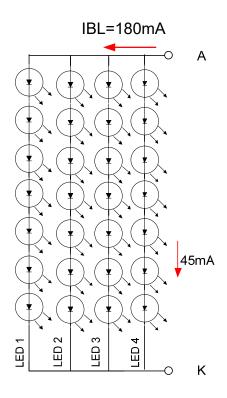
Bmax: The measured maximum luminance of all measurement position.

Bmin: The measured minimum luminance of all measurement position.

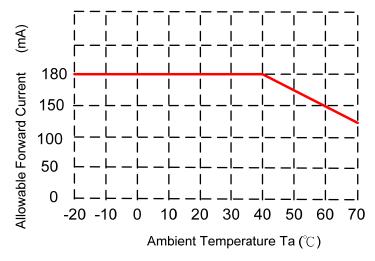
5. Backlight Characteristics

Item	Symbol	Min.	Тур.	Max.	Unit	Condition
LED Backlight Voltage	VBL		21	23.1	V	For reference
LED Backlight Current	IBL	-	180		mA	Ta=25°ℂ
LED Life Time			50K	-	Hrs.	Note*

Note(1) Brightness to be decreased to 50% of the initial value. Ta=25℃



Note(2) When LCM is operated over 40° C ambient temperature, the ILED should be follow :



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6. Electrical Characteristics

6.1 TFT LCD Module Interface Connector

Connector Name / Designation

Item	Description
Manufacturer / Part Number	Starconn / 300E40-0010RA-G3
Mating Model Number	TBD or compatible

Signal Pin Assignment

Pin#	Signal Name	Description
1	VDD	Power Supply Voltage
2	VDD	Power Supply Voltage
3	VDD	Power Supply Voltage
4	NC	No Connection
5	NC	No Connection
6	NC	No Connection
7	NC	No Connection
8	NC	No Connection
9	GND	Ground
10	D2P	MIPI data pair 2 positive signal
11	D2N	MIPI data pair 2 negative signal
12	GND	Ground
13	D1P	MIPI data pair 1 positive signal
14	D1N	MIPI data pair 1 negative signal
15	GND	Ground
16	CLKP	MIPI Clock positive signal
17	CLKN	MIPI Clock negative signal
18	GND	Ground
19	D0P	MIPI data pair 0 positive signal
20	D0N	MIPI data pair 0 negative signal
21	GND	Ground
22	D3P	MIPI data pair 3 positive signal
23	D3N	MIPI data pair 3 negative signal
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	NC	Not Connect
29	NC	Not Connect

30	NC	Not Connect
31	NC	Not Connect
32	NC	Not Connect
33	NC	Not Connect
34	NC	Not Connect
35	BIST	BIST pin. (Keep NC or High if not use.)
36	NC	Not Connect
37	NC	Not Connect
38	VDD_EDID	Power Supply for EDID I2C Flash IC
39	SCL_EDID	I2C Serial Clock for EDID I2C Flash IC
40	SDA_EDID	I2C Serial Data for EDID I2C Flash IC

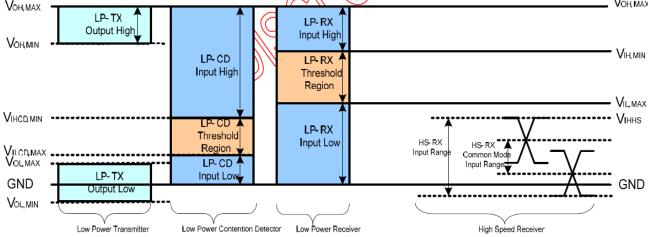
Note: All input signals shall be low or Hi-resistance state when VDD is off.

7. Electrical Characteristics

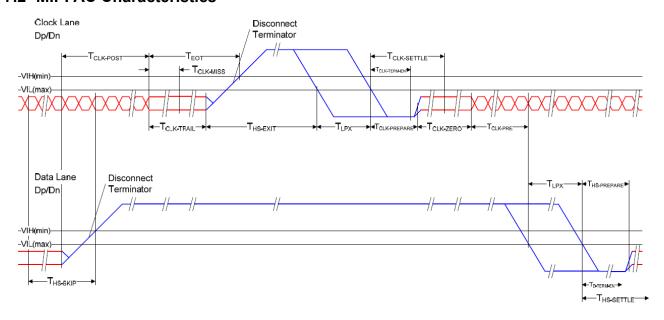
7.1 MIPI DC Characteristics

(VDD=VDDIO=VDD IF=2.3 to 3.6V, VSS=VSSA=VSS IF=0V, TA=-20 to +85°C)

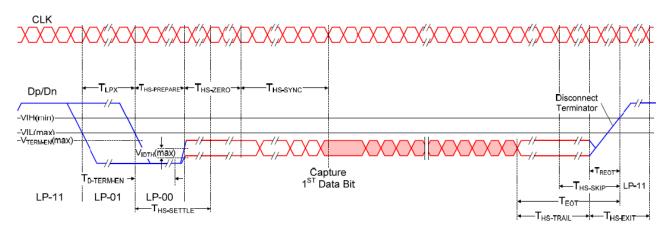
(VDD=VDDIO=VDD_IF=2.	3 10 3.60, 033-0	33A-V33_IF-UV,	TA=-20 to +65 ()		
Parameter	Symbol	Min.	Тур.	Max.	Unit
	MIPI Chara	acteristics for High	Speed Receiver		
Single-ended input low voltage	VILHS	-40	-	-	mV
Single-ended input high voltage	Vihhs	-	-	460	mV
Common-mode voltage	Vcmrxdc	70	-	330	mV
Differential input impedance	Z _{ID}	80	100	125	ohm
HS transmit differential voltage(Vop=Vpp-VpN)	[VOD]	-	200	250	mV
	MIPI Cha	racteristics for Lov	w Power Mode		
Pad signal voltage range	Vı	-50	-11/4	1350	mV
Logic 0 input threshold	VIL	0		550	mV
Logic 1 input threshold	ViH	1000		1350	mV
Output low level	Vol	-50		> 50	mV
Output high level	Vон	(1)	1.2	/ 1.3	V
MIPI Digital Operating Current	IVDDMIPI		15	20	mA
MIPI Digital Stand-by Current	Ізтмірі			250	uA
Vоң мах —	200	(N) \(\sigma \)	ر آبان ا		Vоң
LP-TX Output High		LP- RX Input High			



7.2 MIPI AC Characteristics



Switching the clock lane between clock transmission and low-power mode



Timing of high-speed data transmission in bursts

7.3 MIPI data-clock timing specification

TREOT 30%-85% rise time and fall time 35 r TCLICHISS Time that the transmitter continues to send HS clock after the last associated Data Lane HS-RX. Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of Tr _{E-TRAL} to the beginning of T _{CLIC-TRAL} . Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. TCLICHER Time the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. TIme interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of T _{CLIC-PRE} . Time for the Clock Lane receiver to enable the HS line termination, starting from the ter			9	Spec.		
Time that the transmitter continues to send HS clock after the last associated Data Lane has transitions mitter transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL. Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane has beginning the transition from the 10 HS mode. Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE. Time for the Clock Lane receiver to enable the HS line. Time for the Clock Lane receiver to enable the HS line. Time for the Clock Lane receiver to enable the HS line. Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the time beginning of TLK-PRE. Time interval during which the HS receiver shall ignore any Data Lane HS transitions starting from the beginning of TLK-PRE. Time from start of TLS-TRAIL or TCLK-TRAIL period to start of LP-11 state THS-PREPARE Time from start of TLS-TRAIL or TCLK-TRAIL period to start of LP-11 state THS-PREPARE Time to drive LP-00 to prepare for HS transmission and the transmission than the transmission burst THS-SKIP TIME to drive LP-00 to prepare for HS transmission and the transmission burst THS-SKIP Time to drive flipped differential state after last payload data bit of a HS transmission burst TLPX Length of any Low-Power state period TLPX Ratio of TLPX Ratio of TL	Parameter	Descript	Min.	Тур.	Max.	Unit
Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THE-THAIL to the beginning of TCLK-TRAIL. Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE. Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VILMAX. Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THEPREPARE. Time interval during which the HS receiver shall ignore any Data Lane HS transitions starting from the beginning of THEPREPARE. Time from start of THEPREPARE. Time from start of THEPREPARE. The FREE Attention of THEPREPARE THEPREPARE Time to drive LP-10 to prepare for HS transmission THS-PREPARE THES-PREPARE THES-PREPARE THES-PREPARE Time to drive HS-0 before the Sync sequence THES-SKIP Time to drive LP-00 to prepare for HS transmission THES-TRAIL THES-SKIP Time to drive LP-00 to prepare for HS transmission THS-TRAIL THES-SKIP Time to drive LP-00 to prepare for HS transmission THES-TRAIL THES-SKIP Time to drive LP-00 to prepare for HS transmission THES-REPARE Time to drive LP-00 to prepare for HS transmission THES-REPARE Time to drive LP-00 to prepare for HS transmission THES-TRAIL THES-SKIP Time to drive LP-00 to prepare for HS transmission THES-REPARE Time to drive LP-00 to prepare for HS transmission THES-REPARE Time to drive LP-00 to prepare for HS transmission THES-REPARE TIME to drive LP-00 to prepare for HS transmission THES-REPARE TIME to drive LP-00 to prepare for HS transmission THES-REPARE THES-REPARE TIME to drive LP-00 to prepare for HS transmission THES-TRAIL THES-REPARE THES-REPARE TIME to drive LP-00 to prepare for HS transmission THES-REPARE THES-REPARE TIME to	T _{REOT}	30%-85% rise time and fall time	-	-	35	ns
TCLK-POST*1 clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of The-TRAIL to the beginning of TCLK-TRAIL. TIme that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transmitter prior to Environment P to HS mode. TCLK-SETTLE Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE. Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses value. Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the time point when Dn crosses value. Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of The-PREPARE. Time from start of The-TRAIL of Tcharsal period to start of LP-11 state THS-PREPARE Time from start of The-TRAIL of Tcharsal period to start of LP-11 state THS-PREPARE Time to drive LP-00 to prepare for HS transmission THS-PREPARE Time to drive LP-00 to prepare for HS transmission THS-PREPARE Time to drive LP-00 to prepare for HS transmission THS-SRIP Time-out at RX to ignore transition period of EoT THS-TRAIL Time to drive flipped differential state after last payload data bit of a HS transmission burst TLPX Ratio TLPX Ratio of TLPXMANSTER/TLPS(SLAVE) between Master and Slave side TTAL-GET Time to drive LP-00 after Turnaround Request TTAL-DECT Time to drive LP-00 after Turnaround Request TTAL-DECT Time to drive LP-00 after Turnaround Request TTAL-DECT Time to drive LP-00 after Turnaround Request	T _{CLK-MISS}		-	-	60	ns
TCLK-PRE transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. TCLK-SETTLE Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE. Time for the Clock Lane receiver to enable the HS line termination, starting from the termination, starting from the time point when Dn crosses VILMAX. THIS-SETTLE Time interval during which the HS receiver shall ignore any Data Lane HS transitions starting from the beginning of THIS-PREPARE. TEOT Time from start of THIS-PREPARE. TIME from start of THIS-PREPARE. THIS-PREPARE Time to drive LP-11 lates HS burst 100 receiver the time to drive LP-00 to prepare for HS transmission 40ns + 4*UI - 85ns + 6*UI respectively. THIS-PREPARE Time to drive HS-0 before the Sync sequence 145ns + 10*UI receiver the sequence 145ns + 10*UI	T _{CLK-POST} *1	clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period				ns
TCLK-SETTLE ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE. Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses (Peach - 38 reach - 38 rea	T _{CLK-PRE}	transmitter prior to any associated Data Lane		-		ns
Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of Theoretical period to start of LP-1 state Time from start of The Fall of Toberfall period to start of LP-1 state This-prepare Time to drive LP-10 to prepare for HS transmission 40ns + 4*UI - 85ns + 6*UI required to start of the sequence The prepare time to drive HS-0 before the Sync sequence The prepare time to drive HS-0 before the Sync sequence The prepare time to drive HS transmission 40ns + 4*UI - 55ns + 4*UI required to start of the payload data bit of a HS transmission burst The prepare time to drive HS-0 before the Sync sequence The prepare	T _{CLK-SETTLE}	ignore any Clock Lane HS transitions, starting from the	95	_	300	ns
This-settle ignore any Data Lane HS transitions, starting from the beginning of Thisprepare. Teot Time from start of This-fall or Tolumbul period to start of LP-11 state This-exit if time to drive LP-11 after HS burst This-prepare Time to drive LP-00 to prepare for HS transmission 40ns + 4*UI - 85ns+6*UI requested for the sync sequence This-prepare HS-prepare + Time to drive HS-0 before the Sync sequence This-prepare Time-out at RX to ignore transition period of EoT 40 - 55ns+4*UI requested for HS-transmission burst This-trail Time to drive flipped differential state after last payload data bit of a HS transmission burst The Length of any Low-Power state period 50 requested for the sync state period 50 requested for the sync state period 50	T _{CLK-TERM-EN}	termination, starting from the time point when Dn crosses	reach	-	38	ns
This-prepare to drive LP-00 to prepare for HS transmission 40ns + 4*Ul - 85ns+6*Ul response to the Sync sequence This-prepare to the Sync sequence This-skilp Time-out at RX to ignore transition period of EoT 40 - 55ns+4*Ul response to the Sync to the Sync sequence This-skilp Time to drive flipped differential state after last payload data bit of a HS transmission burst 60 + 4*Ul - response to the Sync to th	T _{HS-SETTLE}	ignore any Data Lane HS transitions, starting from the	85 ns + 6*UI	-	145 ns + 10*UI	ns
Ths-prepare Time to drive LP-00 to prepare for HS transmission 40ns + 4*UI - 85ns+6*UI r Ths-prepare Ths-prepare + Time to drive HS-0 before the Sync sequence 145ns + 10*UI - r Ths-skip Time-out at RX to ignore transition period of EoT 40 - 55ns+4*UI r Ths-trail Time to drive flipped differential state after last payload data bit of a HS transmission burst 60 + 4*UI - r Thy Length of any Low-Power state period 50 - r Ratio Thy Ratio of The Ximaster / The Sichard Details The Sichard 2/3 - 3/2 The The to drive LP-00 by new TX 5*The X The The Sichard The Ximaster The The Ximaster The Ximast	T _{EOT}		-	-	105ns+48*UI	-
Ths-prepare + Time to drive HS-0 before the Sync sequence Ths-prepare + Ths-zero sequence Time-out at RX to ignore transition period of EoT Time to drive flipped differential state after last payload data bit of a HS transmission burst Thy Length of any Low-Power state period Ratio Thy Ratio of The Kimasterial Time to drive LP-00 by new TX The todrive LP-00 after Turnaround Request The sequence 145ns + 10*UI	T _{HS-EXIT} M	time to drive LP-11 after HS burst	100	-	-	ns
+ T _{HS-ZERO} sequence Time-out at RX to ignore transition period of EoT 40 - 55ns+4*UI r T _{HS-TRAIL} Time to drive flipped differential state after last payload data bit of a HS transmission burst 60 + 4*UI - r T _{LPX} Length of any Low-Power state period 50 - r Ratio T _{LPX} Ratio of T _{LPX} (MASTER)/T _{LPS} (SLAVE) between Master and Slave side 7 - 3/2 T _{TA-GET} Time to drive LP-00 by new TX 5*T _{LPX} r T _{TA-GO} Time to drive LP-00 after Turnaround Request 4*T _{LPX} r	T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst TLPX Length of any Low-Power state period Ratio TLPX Ratio of TLPX(MASTER)/TLPS(SLAVE) between Master and Slave side TTA-GET Time to drive LP-00 by new TX TTA-GO Time to drive LP-00 after Turnaround Request 60 + 4*UI r 60 + 4*UI r 7 7 7 7 7 7 7 7 7 7 7 7 7			145ns + 10*UI	-	-	ns
T _{LPX} Length of any Low-Power state period 50 - r Ratio T _{LPX} Ratio of T _{LPX(MASTER)} /T _{LPS(SLAVE)} between Master and Slave side 7 T _{TA-GET} Time to drive LP-00 by new TX 5*T _{LPX} r T _{TA-GO} Time to drive LP-00 after Turnaround Request 4*T _{LPX} r	T _{HS-SKIP}	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
Ratio T _{LPX} Ratio of T _{LPX(MASTER)} /T _{LPS(SLAVE)} between Master and Slave side 2/3 - 3/2 T _{TA-GET} Time to drive LP-00 by new TX 5*T _{LPX} r T _{TA-GO} Time to drive LP-00 after Turnaround Request 4*T _{LPX} r	T _{HS-TRAIL}		60 + 4*UI	-	-	ns
Tale Slave side 2/3 - 3/2	T _{LPX}		50	-	-	ns
T_{TA-GET} Time to drive LP-00 by new TX 5*T _{LPX} r T_{TA-GO} Time to drive LP-00 after Turnaround Request 4*T _{LPX} r	Ratio T _{LPX}		2/3	-	3/2	-
	T _{TA-GET}	Time to drive LP-00 by new TX	5	*T _{LPX}		ns
Transume Time-out before new TX side starts driving Trey - 2*Trey r	T _{TA-GO}	Time to drive LP-00 after Turnaround Request	4	*T _{LPX}		ns
Note: (1) For image transmission:	T _{TA-SURE}	Time-out before new TX side starts driving	T _{LPX} -		2*T _{LPX}	ns

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Note: (1) For image transmission:

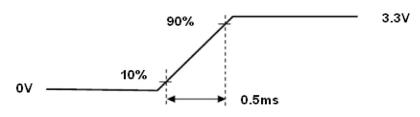
TCLK-POST min value =164 when MIPI max frequency per lane = 0.53Gbps.

TCLK-POST min value =112 when MIPI max frequency per lane = 1Gbps

8. Power Consumption

Item	_	Symbol	Min.	Тур.	Max.	Unit	Note
LCD Drive Voltage		VDD	3.0	3.3	3.6	V	(3)
VDD Current	White Pattern	IDD	-1-	TBD		Α	(2),(3)
VDD Power Consumption	White Pattern	PDD	1	TBD		W	(2),(3)
LED Power Consumption		PLED			8.5	W	(2),(3)

Note (1) Measure Condition



VDD rising time

Note (2) Frame Rate=60Hz, VDD=3.3V, DC Current.

9. Reliability Test Conditions

Test Item	Test Conditions				
High Temperature Operation	70±3°C ,Dry t=240 hrs				
Low Temperature Operation	-20±3°C, Dry t=240 hrs				
High Temperature Storage	80±3°C , Dry t=240 hrs	1,2			
Low Temperature Storage	-30±3°C ,Dry t=240 hrs	1,2			
Storage Humidity Test	60 °C, Humidity 90%, 240 hrs	1,2			
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis				

- Note(1) Condensation of water is not permitted on the module.
- Note(2) The module should be inspected after 1 hour storage in normal conditions (15-35°C, 45-65%RH).
- Note(3) The module shouldn't be tested more than one condition, and all the test conditions are independent.
- Note(4) All the reliability tests should be done without protective film on the module.

10. Use Precautions

10.1 Handling precautions

- (1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- (2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- (3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- (4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

10.2 Installing precautions

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- (1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. $1M\Omega$ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- (2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- (3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- (4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

10.3 Storage precautions

- (1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
- (2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
- (3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

10.4 Operating precautions

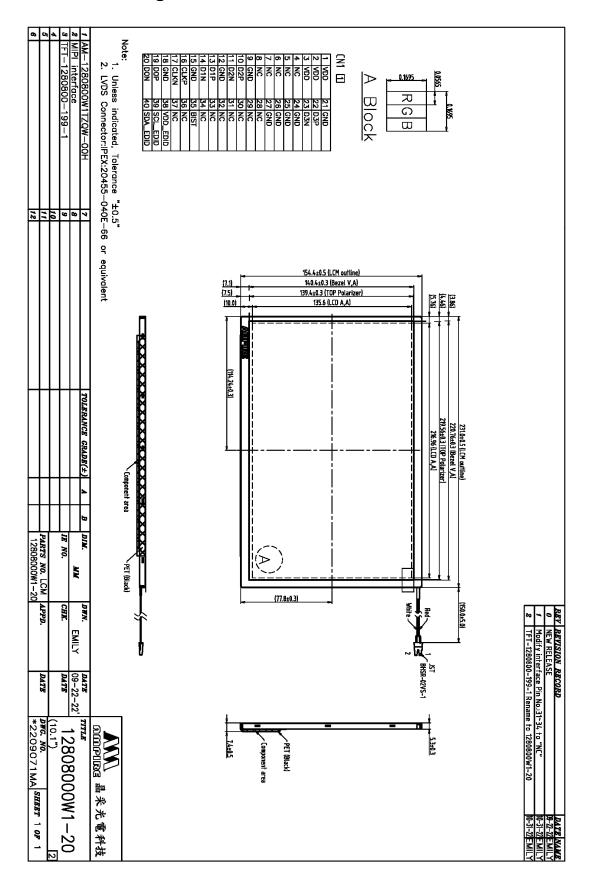
- (1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- (2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- (3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
- (4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- (5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- (6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
- (7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
- (8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

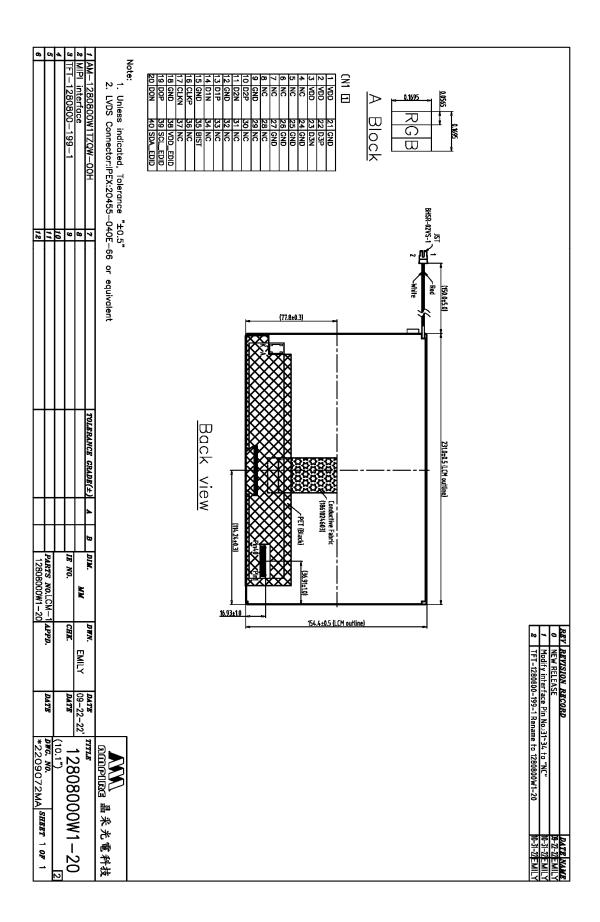
10.5 Other

- (1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- (2) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver.
- (3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

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11. Mechanic Drawing





12. Package TBD